Estd. 1962
"A++" Accredited by NAAC (2021)
With CGPA 3.52

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शिवाजी विद्यापीठ, कोल्हापूर ४१६ ००४, महाराष्ट्र
दूरध्वनी - इपीबीएक्स - २०६०९०००, अभ्यासमंडळे विभाग : ०२३१- २६०९०९४. २६०९४८७
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जा.क्र./शि.वि/अं.म./ 608 दिनांक:— ०७/१०/२०२५

प्रति,

१. मा. संचालक / प्राचार्य,
सर्व संलग्नीत अभियांत्रीकी महाविद्यालये,
शिवाजी विद्यापीठ, कोल्हापूर

२.प्र. संचालक,
स्कुल ऑफ इंजिनिअरींग ॲण्ड टेक्नॉलॉजी,
शिवाजी विद्यापीठ, कोल्हापूर

३.प्र. संचालक,
यशवंतराव चव्हाण स्कुल ऑफ रुरल डेव्हलपमेंट,
शिवाजी विद्यापीठ, कोल्हापूर

विषय:— एम. टेक अभ्यासक्रमातील किरकोळ दुरुस्तीबाबत.

संदर्भ:— १.एसयु/बीओएस/सायन्स&टेक/३१७ व ५३४ दि.२३/५/२०२५ व दि.४/९/२०२५
२.एसयु/बीओएस/सायन्स&टेक/५३९ दि.०८/०९/२०२५

महोदय,

उपरोक्त संदर्भिय विषयास अनुसररुन आपणास आदेशान्वये कळविण्यात येते की, शैक्षणिक वर्ष २०२५—२६ पासून लागू करण्यात आलेल्या खालील **एम.टेक** अभ्यासक्रमामध्ये किरकोळ दुरुस्ती करण्यात आलेली आहे.

Sr.	Course/Syllabus	Sr.	Course/Syllabus
1	Enargy Technology (ON)	6	Rural Technology (ON)
2	Computer Science and Technology (ON)	7	Computer Science and Engineering (OFF)
3	Electronics and Telecommunication (ON)	8	Mechanical (CAD/CAM/CAE) (OFF)
4	Environmental Science and Technology (ON)	9	Electronics and Telecommunication Engineering (OFF)
5	Food Technology (ON)		

सोबत सदर अभ्यासक्रमाची प्रत जोडली आहे. तसेच विद्यापीठाच्या https://www.unishivaji.ac.in (NEP-2020@suk/ Online syllabus) या संकेस्थळावर ठेवण्यात आला आहे. सदर दुरुस्ती ही शैक्षणिक वर्ष २०२५—२६ पासून लागू राहील.

सदर अभ्यासक्रम सर्व संबधित विद्यार्थी व शिक्षकांच्या निदर्शनास आणून द्यावेत ही विनंती.

कळावे.

आपला विश्वासू,

डॉ. एस. एम. कुबल
उपकुलसचिव

सोबत — अभ्यासक्रमाची प्रत,

प्रत :— **माहितीसाठी व पुढील योग्यत्या कार्यवाहीसाठी**

मा. संचालक, परीक्षा व मुल्यमापन मंडळ	प्र. अधिष्ठाता, विज्ञान व तंत्रज्ञान विद्याशाखा
अध्यक्ष, संबंधित अभ्यास /अस्थायी मंडळ	इतर परिक्षा ४ विभागास.
परीक्षक नियुक्ती ए व बी विभागास.	संलग्नता टी. १ व टी. २ विभागास
पीजी प्रवेश विभागास	पीजी सेमिनार विभागास
संगणक केंद्र / आयटी सेल	पात्रता विभागास

Shivaji University

Vidya Nagar, Kolhapur, Maharashtra 416004

Department of Technology

As per NEP2020 guidelines

M. Tech.

(Electronics & Telecommunications) Curriculum Structure and Syllabus

2025-26 onwards

INSTITUTE

VISION:

To be a leader in engineering and technology education, a research centre of global standards to provide valuable resources for industry and society through the development of competent technical human resources.

MISSION:

- To undertake collaborative research projects that offer opportunities for consistent interaction with industries.
- To organize teaching programs to facilitate the development of competent and committed professionals for practice, research and teaching.
- To develop technocrats of international stature committed to the task of nation building.

DEPARTMENT

VISION:

To impart quality technical education to students through research, innovation and teamwork for a lasting technology development in the area of Electronics and Communication Engineering and to become an exemplary professional of high ethics.

MISSION:

To provide exposure of research , technological developments and hands on experience of project development in Electronics engineering to the students by Emphasizing active Learning with Strongly Supported Laboratory Component and to prepare them for Professional Careers

Program Outcomes

1. Scholarship of Knowledge: The ability to acquire and synthesize in-depth, specialized knowledge, including a global perspective, to enhance one's understanding of the discipline.

2. Critical Thinking: The ability to critically analyse complex engineering problems and apply independent judgment to make intellectual and creative advances in a broader theoretical, practical, and policy context.

3. Problem Solving: The ability to think laterally and originally to solve engineering problems. This involves evaluating a wide range of solutions, while considering public health and safety, societal, and environmental factors.

4. Research Skill: The ability to use literature surveys and experiments to extract information, apply appropriate methodologies and tools, and analyze data to contribute to scientific and technological knowledge.

5. Usage of Modern Tools: The ability to select and apply modern engineering and IT tools, including modelling and prediction, with an understanding of their limitations.

6. Collaborative and Multidisciplinary Work: A knowledge of group dynamics and the capacity for self-management, teamwork, and decision-making to contribute positively to multidisciplinary research and achieve common goals.

7. Project Management and Finance: The ability to apply engineering and management principles to manage projects efficiently in a multidisciplinary environment, considering financial and economic factors.

8. Communication: The ability to communicate complex engineering activities confidently and effectively with both the engineering community and society. This includes writing

reports, giving presentations, and giving clear instructions.

9. Life-long Learning: A recognition of the need for, and the ability to engage in, independent and continuous life-long learning to improve competence.

10. Ethical Practices and Social Responsibility: Professional and intellectual integrity, a commitment to a code of conduct and ethics of research, and an understanding of the impact of research outcomes on the community and sustainable development.

Program Educational Objectives

1) Development of skilled technocrats by encouraging students to acquiring engineering knowledge and communication skills.

2) To develop an ability among the students to provide the solution on specific problem within realistic constraints.

3) To encourage students for excellence in research, academics, higher studies, administration, entrepreneurship, leadership and other areas to serve the nation.

4) To develop students with high integrity, character and moral ethics.

SHIVAJI UNIVERSITY, KOLHAPUR
Department of Technology
M. Tech. Electronics & Telecommunication Course Structure
Semester-I
Applicable From Academic Year 2025-26

Sr. No	Subject Code	Subject Title	Teaching Scheme (Hours/week)				Examination Scheme			
							Theory		Practical	
			L	T	P	Credits	Scheme	Max. marks	Scheme	Max. marks
1	METCAC1	Research Methodology	2	-	-	2	--	--	IOE	50
									--------	-------
2	METCC11	ASIC's and FPGA	3	-	-	4	ISE	40	--------	-------
							ESE	60	--------	-------
3	METCC12	Advance Computer Networks	3	-	-	3	ISE	40	--------	-------
							ESE	60	--------	-------
4	METCC13	Microwave Theory and Circuits	3	-	-	3	ISE	40	--------	-------
							ESE	60	--------	-------
5	METCE11	**Elective-I:**	3		-	3	ISE	40	--------	-------

							ESE	60	--------	-------
6	METCOE12	Elective- II (Open Elective)	3	-	-	3	ISE	40		
							ESE	60		
7	METCC14	Seminar-I	--		2	1	----	----	IOE	50
8	METCC15	Laboratory- I : Advance Computer Network	-	-	2	1	--------	-------	IOE	50
9	METCC16	Laboratory-II : Microwave theory and circuits lab	-	-	2	1	--------	-------	IOE	50
		Total	**17**	**-**	**6**	**20**		**500**		**200**
Total Contact hours per week =23*										

Elective –I
1. Advanced Antenna Theory and Application.
2. Design of Micro strip Antennas
3. Computational Electromagnetics

Elective II (Open Elective): choose from list on next page

*** Students from M. Tech any branch of the Department of Technology Can opt for this Elective.**

Semester –I (Open Elective*)

Sr. No.	Elective-II (Open Elective*)	Branch
1	**METCOE11 Advanced Communication System**	**Electronics & Telecommunication**
2	**METCOE12 Reconfigurable Computing**	
3	**METCOE13 VLSI Testing & Testability**	
4	**FTE-21:Advances in processing of dairy Technology**	**Food Technology**

5	FTE-22: Food Trade Management	
6	FTE-23: Advances in Grain Science and Technology	
7	ETOE11: Electric Vehicles and Renewable Energy	Energy Technology
8	ETOE12: Energy Efficient Buildings	
9	ETOE13: Computational Fluid Dynamics	
10	ESTE-21 Environmental Biotechnology	Environmental Science and Technology
11	ESTE-22 Energy Efficient Building	
12	ESTE-23 Operational Health and Safety Management	
13	CSTEOE1: Advanced Operating Systems	Computer Science and Technology
14	CSTOE2: Internet of Things	
15	CSTOE3: Data Analytics	

Minimum number of students for selection of Elective - 4

Maximum number of students for selection of Elective - 24 *

***Preference will be given to core branch**

SHIVAJI UNIVERSITY, KOLHAPUR
Department of Technology
M. Tech. Electronics & Telecommunication Course Structure
Semester-II
Applicable From Academic Year 2025-26

Sr. No	Subject Code	Subject Title	Teaching Scheme (Hours/week)				Examination Scheme	
							Theory	Practical

			L	T	P	Credits	Scheme	Max. marks	Scheme	Max. marks
1	ETCAC2	Intellectual Property Rights	**2**	**-**	**-**	**2**	**----**	**---**	**IOE**	**50**
2	METCC21	Real Time Operating Systems	3	-	-	3	ISE	40	--------	-------
							ESE	60	--------	-------
3	METCC22	Advanced Embedded System	3	-	-	3	ISE	40	--------	-------
							ESE	60	--------	-------
4	METCC23	Advance Mobile Systems	3	-	-	3	ISE	40	--------	-------
							ESE	60	--------	-------
5	METCE21	Elective-III	3	-	-	3	ISE	40	--------	-------
							ESE	60	--------	-------
6	METCOE22	Elective- IV (Open Elective)	3	-	-	3	ISE	40		
							ESE	60		
7	METCC24	Seminar	-	-	2	1	--------	-------	IOE	50
8	METCC25	Laboratory- I : Real Time Operating System Lab	-	-	2	1	--------	-------	IOE	50
9	METCC26	Laboratory-II : Advance Mobile system lab	-	-	2	1	--------	-------	IOE	50
		Total	**17**	**-**	**6**	**20**		**500**		**200**
Total Contact hours per week =23*										

Elective-III
1. SoC Design
2. Multimedia Systems
3. Robotics and Automation
4. Advanced Computer Architecture

Semester –II (Open Elective*)

Sr. No.	Elective-IV (Open Elective*)	Branch
1	METCOE21: MIMO Systems	Electronics & Telecommunication
2	METCOE22: Satellite Communication	
3	METCOE23:Smart and Phased Array Antenna Design	
4	FTE-41: Recent developments in processing of plantation crops	Food Technology
5	FTE-42: Project Management for Food Processing Industries	
6	FTE-43: Sustainable Food Process Engineering	
7	ETOE21 : Energy Modeling and Project Management	Energy Technology
8	ETOE22 : Artificial Intelligence in Energy Systems	
9	ETOE23 : Design and Optimization of Energy Systems	
10	ESTE-41 Operation and Maintenance of Environmental Facilities	Environmental Science and Technology
11	ESTE-42 Rural Water Supply and Sanitation	
12	ESTE-43 Emerging Technologies in Water and Wastewater Treatment	
13	CSTOE21: Geographical Information Systems	Computer Science and Technology
14	CSTOE22: Natural Language Processing	
15	CSTOE23: Blockchain Technology	

Minimum number of students for selection of Elective - 4
Maximum number of students for selection of Elective - 24 *

***Preference will be given to core branch**

SHIVAJI UNIVERSITY, KOLHAPUR
Department of Technology
M. Tech. Electronics & Telecommunication Course Structure
Semester- III
Applicable From Academic Year 2025-26

Sr. No	Subject Code	Subject Title	Teaching Scheme (Hours/week)				Examination Scheme			
							Theory		Practical	
			L	T	P	Credits	Scheme	Max. marks	Scheme	Max. marks
2	METCC31	Industrial Training	-	-	2*	5**	--------	-------	IOE	50
									EOE	50
3	METCC32	Dissertation Phase-I	-	-	2*	15	--------	-------	IOE	100
									EOE	100
		Total	-	-	4	20				300
Total Contact hours per week =4*										

*Students are expected to do self-study for two hours as per the guidance given by the

Project Guide and report to the department once a week. Hence contact hours to be taken as two for the calculation of contact hours.

** Industrial Training of Eight weeks at the end of First Year

OR

Industrial training will be split in two slots of four weeks during semester III

Evaluation at end of III semester on the basis given report and Presentation to concern Guide.

SHIVAJI UNIVERSITY, KOLHAPUR
Department of Technology
. M.Tech. Electronics & Telecommunication Course Structure
Semester- IV
Applicable From Academic Year 2025-26

Sr. No.	Subject Code	Subject Title	Teaching Scheme (Hours/week)				Examination Scheme			
							Theory		Practical	
			L	T	P	Credits	Scheme	Max. marks	Scheme	Max. marks
1	METCC41	Dissertation Phase-II	-	-	4*	20	---	---	IOE	100
									EOE	200
		Total	-	-	4	20	----	--		300
Total Contact hours per week =4*										

*Students are expected to do self-study for two hours as per the guidance given by the project Guide and report to the department once in a week. Hence contact hours to be taken as two for the calculation of contact hours.
Note:

$: Minimum 40% marks required in SEE as passing head.

• Tutorials and practical shall be conducted in batches with batch strength not exceeding 18 students.

ISE –In Semester Examination, ESE – End Semester Examination,

IPE – Internal Practical Evaluation, EPE–External Practical Examination,

IOE– Internal Oral Evaluation, EOE–External Oral Examination

SEMESTER-I

<table>
<tr><td>Class, Part & Semester</td><td>:</td><td colspan="5">First Year M. Tech (E&TC), Part I, Sem-I</td></tr>
<tr><td>Course Title</td><td>:</td><td colspan="3">Research Methodology</td><td>Course Code:</td><td>:</td><td>METCAC1</td></tr>
<tr><td rowspan="2">Teaching Scheme (Hours)</td><td rowspan="2">:</td><td>Lecture :</td><td colspan="2">2 Hrs/week</td><td rowspan="2">Total Credits</td><td rowspan="2">:</td><td rowspan="2">2</td></tr>
<tr><td>Tutorial :</td><td colspan="2">-- Hrs/week</td></tr>
<tr><td>Evaluation Scheme (Marks)</td><td>:</td><td>IOE= 50</td><td>ESE = NIL</td><td>Grand Total=50</td><td>Duration of ESE</td><td>:</td><td>—</td></tr>
<tr><td>Revision:</td><td>:</td><td colspan="3">Fourth</td><td>Month</td><td>:</td><td>July 2025</td></tr>
<tr><td>Pre-requisites (if any)</td><td>:</td><td colspan="6">Not required</td></tr>
<tr><td>Course Domain</td><td>:</td><td colspan="6">Research Theory</td></tr>
<tr><td colspan="8">Course Rationale: This course aims to lay a foundation for your research. The goal is to help you to design and develop your future research projects.</td></tr>
<tr><td colspan="4">Course Objectives: The Course teacher will</td><td colspan="4">Course Outcomes: Students will be able to</td></tr>
<tr><td>1.</td><td colspan="3">This course aims to lay a foundation for your research. The goal is to help you to design</td><td>1.</td><td colspan="4">To understand basic concepts of research and its methodologies</td></tr>
</table>

	and develop your future research projects.		
2.	Familiarize Research Design.	2.	To select and define appropriate research problem and parameters
3.	Introduce measurement and scaling techniques in research.	3.	To apply Measurement and Scaling Techniques
4.	Familiarize methods of data collection and analysis	4.	To use Methods of Data Collection and Analysis
5.	Introduce techniques of hypotheses, parametric or standard tests	5.	To apply techniques of hypotheses, parametric or standard tests
6.	Help to analyze variance and co-variance	6.	Present and defend research ideas using Analysis of Variance and Co-variance

Curriculum Content	**Hours**
Unit I Research Methodology: An Introduction, Objectives of Research, Types of Research, Research Methods and Methodology, Defining a Research Problem, Techniques involved in Defining a Problem	5
Unit II Research Methodology: An Introduction Objectives of Research, Types of Research, Research Methods and Methodology, Defining a Research Problem, Techniques involved in Defining a Problem	5
Unit III Measurement and Scalin Techniques Measurement in Research, Measurement Scales, Sources in Error, Techniques of Developing Measurement Tools, Scaling, Meaning of Scale, Scale Construction Techniques.	4
Unit IV Methods of Data Collection and Analysis Collection of Primary and Secondary Data, Selection of appropriate method, Data Processing Operations, Elements of Analysis, Statistics in Research, Measures of Dispersion, Measures of Skewness, Regression Analysis, Correlation	4
Unit V Techniques of Hypotheses, Parametric or Standard Tests Basic concepts, Tests for Hypotheses I and II, Important parameters, Limitations of the tests of Hypotheses,. Chi-square Test, Comparing Variance, As a non-parameteric Test, Conversion of Chi to Phi, Caution in using Chi-square test	4
Unit VI Analysis of Variance and Co-variance ANOVA, One way ANOVA, Two Way ANOVA, ANOCOVA, Assumptions in ANOCOVA, Multivariate Analysis Technique, Classification of Multivariate Analysis,	5

factor Analysis, R-type Q Type factor Analysis, Path Analysis	
Suggested list of Tutorials and Assignments: As suggested by the course teacher	
Suggested Text Books:	
1.	"Research Methodology", C.R. Kothari, Wiley Eastern.
2.	
Suggested Reference Books:	
1.	"Formulation of Hypothesis", Willkinson K.P, L Bhandarkar, Hymalaya Publication, Bombay.
2.	"Research in Education", John W Best and V. Kahn, PHI Publication.
3.	"Research Methodology- A step by step guide for beginners", Ranjit Kumar, Pearson Education
4.	"Management Research Methodology-Integration of principles, methods and Techniques", K.N. Krishnaswami and others, Pearson Education
5.	

Course Outcome and Program Outcome Mapping

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10
CO 1			2							
CO 2				3						
CO 3				2						
CO 4	2			3						
CO 5				3						
CO6				3						2

Level of Mapping as: Low 1, Moderate 2, High 3

Class, Part & Semester	:	**First Year M. Tech (E&TC), Part I, Sem-I**					
Course Title	:	ASIC's and FPGA			***Course Code*:**	:	METCC11
Teaching Scheme (Hours)	:	Lecture :	3 Hrs/week		***Total Credits***	:	3
		Tutorial :	-- Hr/week				
Evaluation Scheme (Marks)	:	ISE=40	ESE = 60	Grand Total=100	***Duration of ESE***	:	3 hrs
Revision:	:	Fourth			***Month***	:	July 2025

Pre-requisites *(if any)*	**:**	Digital Systems and Circuit Design
Course Domain	**:**	Embedded

Course Rationale: ASICs are custom-designed for specific applications, offering high performance and efficiency, while FPGAs are reprogrammable and versatile, suitable for prototyping and applications requiring flexibility.

Course Objectives: The Course teacher will		***Course Outcomes:*** Students will be able to	
7.	To familiarize the use of hardware description language in ASIC & FPGA.	**7.**	To understand the VHDL language & its programming.
8.	To introduce the various types of ASICs its design how & various programmable logic device.	**8.**	To understand the ASICs & FPGAS & the implementation of digital logic these devices.
9.	To familiarize the FPGA & implementation of digital logic on programmable logic devices.	**9.**	To understand the concept of FPGA, various types of FPGAS & its architecture.
10.	To introduce the physical design algorithms and role of testing in VLSI design.	**10.**	To understand physical design algorithms & various testing techniques.

Curriculum Content	**Hours**
Unit I **Introduction to hardware description languages:** Introduction to VHDL, types of modelling, dataflow modelling, behavioural modelling, structural modelling, use of package for structural modelling, finite state machine modelling.	6
Unit II **Introduction to ASICs:** Introduction to ASICs, ASIC design flow, types of ASICs, full custom ASIC's, standard cell based ASIC's, Gate array based ASIC's, channelled gate array, structured gate arrays, programmable logic devices, introduction to programmable logic, fixed versus programmable logic, programmable logic devices, types of programmable logic devices, PROMs, PLA, PAL, CPLD & FPGA.	7
Unit III **Introduction to FPGA** Introduction to FPGA, evolution of programmable devices conceptual diagram of a typical FPGA, Logic blocks, interconnection resources, FPGA versus ASIC, applications of FPGA, FPGA design flow, and implementation process	7
Unit IV **FPGA Architecture** various classes of FPGAs, symmetrical array, row-based, hierarchical PLD, sea-of-gates. Programming technologies, static RAM programming technology, anti-fuse programming technology, EPROM and EEPROM programming technology, commercially available FPGAs, general architecture of Xilinx FPGAS, CLB Interconnect.	7

Unit V **Physical Design** Circuit partitioning algorithm, K-L algorithm, floor planning algorithm, cluster growth roof planning, introduction to placement & routing.	6
Unit VI **VLSI Testing** Basic concepts to testing, yield and reject rate, ATPG, ATPG design flow, various stuck at faults BIST.	7
Suggested list of Tutorials and Assignments: As suggested by the course teacher	

Suggested Text Books:	
1.	M.J.S. Smith,"ApplicationSpecific Integrated Circuits", Pearson, 2003
2.	2. H.Gerez, "Algorithms for VLSI Design Automation", John Wiley,1999
3.	
Suggested Reference Books:	
1.	FPGA Prototyping by VHDL Examples (Xilinx Spartan 3 Version) by Pong P. Chu (Pub: Wiley)
2.	Synthesis of Arithmetic Circuits- FPGA, ASIC and Embedded Systems by Jean-Pierre Deschamps, Gery Jean Antoine Bioul and Gustavo D. Sutter
3.	Verilog by Example: A Concise Introduction for FPGA Design by Blaine Readler (Pub: Full Arc Press).
4.	Laung-Terng Wang, Charles E. Stroud, Nur A. Touba, "System-on-chip Test Architectures: Nanometer Design for Testability", 2008, Morgan Kaufmann Publishers
5.	Xilinx ISE User guide, available online, also along with s/w installation.
6.	

Course Outcome and Program Outcome Mapping

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10
CO 1			3		2					
CO 2	2									
CO 3				2						
CO 4		2	3							
CO 5										
CO6										

Level of Mapping as: Low 1, Moderate 2, High 3

Class, Part & Semester	**:**	**First Year M. Tech (E&TC), Part I, Sem-I**					
Course Title	**:**	**Advance Computer Networks**			***Course Code*:**	**:**	METCC12
Teaching Scheme (Hours)	**:**	Lecture :	3 Hrs/week		***Total Credits***	**:**	3
		Tutorial :	-- Hrs/week				
Evaluation Scheme (Marks)	**:**	ISE=40	ESE = 60	Grand Total=100	***Duration of ESE***	**:**	3 hrs
Revision:	**:**	Fourth			***Month***	**:**	July 2025
Pre-requisites *(if any)*	**:**	Not required					
Course Domain	**:**	**Communication**					

Course Rationale: This course aims to equip students with a strong understanding of networking principles, protocols, and technologies, enabling them to design, implement, and manage computer networks, including LANs, WANs, and the Internet.

Course Objectives:		***Course Outcomes:*** Students will be able to	
11.	To explain the concepts of OSI model and protocol architecture	11.	Understand network communication using the layered concept, Open System Interconnect (OSI) and the Internet Model.
12.	To demonstrate the detailed inner workings of TCP/IP protocol suite	12.	Learn various types of transmission media, network devices; and parameters of evaluation of performance for each media and device.
13.	To discuss data link layer design issues and MAC sub layer protocols	13.	Analyze the concept of flow control, error control and LAN protocols; to explain the design of, and algorithms used in, the physical, data link layers.
14.	To demonstrate Network layer design issues, various routing algorithms and congestion control algorithms	14.	Demonstrate the working principles of LAN and the concepts behind physical and logical addressing, subnetting and supernetting.
15.	To explain transport layer protocols and application layer	15.	Understand the functions performed by a Network Management System and to analyze connection establishment and congestion control with respect to TCP Protocol.
16.		16.	Demonstrate the principles and operations behind various application layer protocols like HTTP, SMTP, FTP.

Curriculum Content	**Hours**
Unit I Introduction to ISO-OSI, TCP-IP and the Internet, ISPs and Internet Backbones. Transport-Layer Services, Relationship Between Transport and Network Layers, Overview of the Transport Layer in the Internet, Connectionless Transport: UDP, UDP Segment Structure, UDP Checksum, Principles of Reliable Data Transfer, Building a Reliable Data Transfer Protocol, Pipelined Reliable Data Transfer Protocols, Go-Back-N (GBN), Selective Repeat (SR),	7
Unit II Connection-Oriented Transport: TCP, The TCP Connection, TCP Segment Structure, Round Trip Time Estimation and Timeout, Reliable Data Transfer, Flow Control, TCP Connection Management, Principles of Congestion Control, The Causes and the Costs of Congestion, Approaches to Congestion Control, Network-Assisted Congestion-Control Example: ATM ABR Congestion Control, TCP Congestion Control,	6
Unit III The Internet Protocol (IP): Forwarding and Addressing in the Internet, Datagram Format, IPv4, Addressing, Internet Control Message Protocol (ICMP), mobile IP, Network Switching, Virtual Circuit and Datagram Networks, Data Forwarding and Routing, **Routing Algorithms, ARP, DHCP.**	7
Unit IV IPv6 Introduction, IP6 Addresses, Mobile IP6, IP6 Transition mechanism. IP switching and Multiprotocol Label Switching (MPLS), Overview of IP over ATM and its evolution to IP switching. MPLS architecture and framework. MPLS Protocols. Traffic Engineering issues in MPLS.	7
Unit V Framing; error control, error detection, parity checks, Internet Checksum and Cyclic Redundancy Codes for error detection; Flow control, ARQ strategies and their performance analysis using different distributions; HDLC protocol. Media Access Control (MAC): MAC for wired Local Area Networks (LAN), Wireless and Mobile Networks: Introduction, Wireless Links and Network Characteristics: CDMA, iFi:802.11 Wireless LANs: The 802.11 Architecture, The 802.11 MAC Protocol, Personal Area Networks: Bluetooth and Zigbee, Cellular Internet Access,: An Overview of Cellular Network Architecture, 3G Cellular Data Networks: Extending the Internet to Cellular subscribers, On to 4G: LTE, Mobility Management:	7
Unit VI Selected Application Layer Protocols: Web and HTTP, electronic mail (SMTP), file transfer protocol (FTP), Domain Name Service (DNS). Real-Time Traffic, Voice Over IP and Multimedia. Design issues in protocols at different layers, Session, Presentation, and Application Layers. Examples: DNS, SMTP, IMAP, HTTP, etc Network Management: What Is Network Management?, The Infrastructure for Network	6

Management, SNMP Protocol Operations and Transport Mappings, Security and Administration,	
Suggested list of Tutorials and Assignments: As suggested by the course teacher	
Suggested Text Books:	
1.	Data communication and Networking. -B.A. Forouzen, 4th Edition TMH.
2.	TCP/IP Protocol Suit - B.A. Forouzen, 4th Edition TMH.
3.	
Suggested Reference Books:	
1.	Wireless Communication System -Abhishek yadav –University Sciences Press, 2009.
2.	Andrew .S. Tanenbaum, "Computer Networks", 4th Edition, Prentice Hall of India, New Delhi, 2008. .
3.	High Performance TCP-IP Networking -Mahaboob Hassan -Jain Raj-PHI.
4.	Fred Halsall, "Data Communications and Networking", 5th Edition, McGraw Hill, 2012.

Course Outcome and Program Outcome Mapping

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10
CO 1	2	3	3							
CO 2		3	3							
CO 3		2								
CO 4			2							
CO 5							3			
CO6				4						

Level of Mapping as: Low 1, Moderate 2, High 3

Class, Part & Semester	**:**	**First Year M. Tech (E&TC), Part I, Sem-I**					
Course Title	**:**	**Microwave Theory and Circuits**			***Course Code*:**	**:**	METCC13
Teaching Scheme (Hours)	**:**	Lecture :	3 Hrs/week		***Total Credits***	**:**	3
		Tutorial :	-- Hrs/week				
Evaluation Scheme (Marks)	**:**	ISE=40	ESE = 60	Grand Total=100	***Duration of ESE***	**:**	3 hrs
Revision:	**:**	Fourth			***Month***	**:**	July 2025
Pre-requisites *(if any)*	**:**	Microwaves					

Course Domain	**:**	Communication

Course Rationale: The course will be broadly focusing on analysis, design and development of microwave circuits and systems. The course will cover introduction to Microwaves, Microwave transmission modes, Transmission lines, Impedance Matching, Microwave Network Analysis, Directional Coupler, Power Divider, Microwave Filters, Microwave Attenuator, RF switches and phase shifters, Microwave Amplifiers, Low Noise Amplifier, Microwave Mixers and Oscillators.

Course Objectives: The Course teacher will		***Course Outcomes:*** Students will be able to	
17.	Explain Microwave transmission lines	17.	Understand Waveguides and transmission lines.
18.	Explain Impedance matching, smith chart and power dividers and combiners	18.	Understand Impedance matching, smith chart and power dividers and combiners
19.	Explain Diodes and Attenuators, RF Switches, Phase Shifters	19.	understand Diodes and Attenuators, RF Switches, Phase Shifters
20.	Teach microwave amplifier design, LNA design.	20.	Students shall learn how to design microwave amplifier design, LNA
21.	Teach Microwave oscillator and mixer design	21.	Shall learn how to design Microwave oscillator and mixer .

Curriculum Content	**Hours**
Unit I Introduction to Microwaves: History and Applications, Effect of Microwaves on human body Microwave Transmission Modes, Waveguides, Transmission Lines	5
Unit II Smith Chart, Impedance Matching, ABCD and S-Parameters Power dividers, Combiners, Couplers	7
Unit III Microwave Filters	7
Unit IV Microwave Diodes and Attenuators, RF Switches, Phase Shifters	7
Unit V Microwave Transistors, Amplifiers and LNA Power Amplifiers and Microwave Tubes	8
Unit VI Microwave Oscillators and Mixers	7

Suggested list of Tutorials and Assignments: As suggested by subject teacher

Suggested Text Books:	
1.	Microwave theory and techniques by Prof Girish Kumar
Suggested Reference Books:	

Course Outcome and Program Outcome Mapping

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10
CO 1	1	1	1	1				1		
CO 2	1	1	1	1	1			1		
CO 3	1	1	1	1				1		
CO 4		1	1	1	1	1		1	1	
CO 5		1	1	1	1	1		1	1	
CO6										

Level of Mapping as: Low 1, Moderate 2, High 3

Elective-I

Class, Part & Semester	**:**	**First Year M. Tech (E&TC), Part I, Sem-I**					
Course Title	**:**	**Advanced Antenna Theory and Application (Elective-I)**			***Course Code*:**	**:**	METCE11
Teaching Scheme (Hours)	**:**	Lecture :	3 Hrs/week		***Total Credits***	**:**	3
		Tutorial :	-- Hrs/week				
Evaluation Scheme (Marks)	**:**	ISE=40	ESE = 60	Grand Total=100	***Duration of ESE***	**:**	3 hrs
Revision:	**:**	Fourth			***Month***	**:**	July 2025
Pre-requisites *(if any)*	**:**	Antenna Theory					
Course Domain	**:**						

Course Rationale: In this subject students shall learn the basic antenna parameters, how to draw antenna radiation patterns, how to calculate, Directivity, Gain, Antenna efficiency, Beam efficiency, Bandwidth. They shall learn Linear Wire Antennas, Region separation, Finite length dipole, half wave dipole and Ground effects. They shall study various types of loop antennas and Linear arrays. They shall study various types of aperture antennas, horn antennas, Microstrip antennas and horn antennas.

Course Objectives: The Course teacher will		***Course Outcomes:*** Students will be able to	
22.	**Teach** the basic antenna parameters, how to draw antenna radiation patterns, how to calculate, Directivity, Gain, Antenna efficiency, Beam efficiency, Bandwidth etc.	**22.**	To draw antenna radiation patterns, to calculate, Directivity, Gain, Antenna efficiency, Beam efficiency, Bandwidth
23.	**Explain** Linear Wire Antennas, Region separation, Finite length dipole, half wave dipole and Ground effects.	**23.**	**Learn** Linear Wire Antennas, Region separation, Finite length dipole, half wave dipole and Ground effects.
24.	Explain various types of loop antennas and Linear arrays.	**24.**	They shall study various types of loop antennas and Linear arrays.
25.	Explain various types of aperture antennas, horn antennas, Microstrip antennas and horn antennas.	**25.**	Know various types of aperture antennas, horn antennas, Microstrip antennas and horn antennas.
26.		**26.**	

Curriculum Content	**Hours**
Unit I **Introduction:** Types of Antennas – Wire antennas, Aperture antennas, Micro strip antennas, Array antennas Reflector antennas, Lens antennas. Radiation Mechanism, Current distribution on thin wire antenna	6
Unit II **Fundamental Parameters of Antennas**: Radiation Pattern, Radiation Power Density, Radiation Intensity, Directivity, Gain, Antenna efficiency, Beam efficiency, Bandwidth, Polarization, Input Impedance, radiation efficiency, Antenna Vector effective length, Friis Transmission equation, Antenna Temperature.	7
Unit III Linear Wire Antennas: Infinitesimal dipole, Small dipole, Region separation, Finite length dipole, half wave dipole, Ground effects	7
Unit IV **Loop Antennas:** Small Circular loop, Circular Loop of constant current, Circular loop with non uniform current. **Linear Arrays:** Two element array, N Element array: Uniform Amplitude and spacing, Broadside and End fire array, Super directivity, Planar array, Design consideration.	7
Unit V	7

Aperture Antennas: Huygen's Field Equivalence principle, radiation equations, Rectangular Aperture, Circular Aperture. **Horn Antennas:** E-Plane, H-plane Sectoral horns, Pyramidal and Conical horns**.**	
Unit VI **Micro strip Antennas:** Basic Characteristics, Feeding mechanisms, Method of analysis, Rectangular Patch, Circular Patch. **Reflector Antennas:** Plane reflector, parabolic reflector, Cassegrain reflectors.	7
Suggested list of Tutorials and Assignments:	
Suggested Text Books:	
1.	
Suggested Reference Books:	
1.	Constantine A. Balanis, "Antenna Theory Analysis and Design", John Wiley & Sons, 2nd edition
2.	John D Kraus, Ronald J Marhefka, Ahmad S Khan, "Antennas for All Applications", Tata McGraw- Hill, 2002
3.	R.C.Johnson and H.Jasik, "Antenna Engineering hand book", Mc-Graw Hill, 1984
4.	I.J. Bhal and P.Bhartia, "Micro-strip antennas", Artech house, 1980
5.	
6.	

Course Outcome and Program Outcome Mapping

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10
CO 1	1	1	1	1	1	1	1	1		
CO 2	1	1	1	1	1	1	1	1		
CO 3	1	1	1	1	1	1	1	1		
CO 4	1	1	1	1	1	1	1	1		
CO 5										
CO6										

Level of Mapping as: Low 1, Moderate 2, High 3

Class, Part & Semester	**:**	**First Year M. Tech (E&TC), Part I, Sem-I**				
Course Title	**:**	**Design of Micro strip Antenna (Elective-I)**		***Course Code*:**	**:**	METCE12
Teaching	**:**	Lecture :	3 Hrs/week	***Total Credits***	**:**	3

Scheme (Hours)		Tutorial :	-- Hrs/week				
Evaluation Scheme (Marks)	**:**	ISE=40	ESE = 60	Grand Total=100	***Duration of ESE***	**:**	3 hrs
Revision:	**:**	Fourth		***Month***	**:**	July 2025	
Pre-requisites *(if any)*	**:**	Antenna Theory					
Course Domain	**:**	Communication					

Course Rationale: Microstrip antennas (MSAs) have several advantages, including that they are lightweight and small-volume and that they can be made conformal to the host surface. In addition, MSAs are manufactured using printed-circuit technology, so that mass production can be achieved at a low cost.

Course Objectives: The Course teacher will		***Course Outcomes:*** Students will be able to	
27.	Explain theory, various parameters of Antennas.	**27.**	Design and test BW, Radiation pattern, input impedance of RMSAs
28.	Explain design procedure of antennas.	**28.**	Design and test BW, Radiation pattern of Planar Multi resonator Broadband MSAs.
29.	Explain how to measure various parameters of antennas such as BW, radiation pattern etc. If there is mismatch between desired parameters and obtained parameters of antenna, then how to resize antenna to get desired BW ,radiation pattern etc.	**29.**	Design and test BW, Radiation pattern of Multilayer Broadband MSAs
30.	Explain to how to design and test RMSAs, Planar Multi resonator Broadband MSAs, Multilayer Broadband MSAs, stacked multi resonator MSAs, compact broadband multi resonator MSAs, Broadband circularly polarised MSAs.	**30.**	Design and test BW, Radiation pattern of stacked multi resonator MSAs, compact broadband multi resonator MSAs.
31.		**31.**	Design and test BW, Radiation pattern of Tunable and dual band MSAs, Broadband circularly polarized MSAs.

Curriculum Content	**Hours**
Unit I Introduction, Characteristics of MSAs, Advantages, Disadvantages and Applications of MSAs. Feeding Techniques, Methods of Analysis, Definition of BW Modified Shape Patches, Planar Multi resonator Configurations, Multilayer Configurations, Stacked Multi resonator MSAs, Impedance-Matching Networks for Broadband MSAs.	6
Unit II **Regularly Shaped Broadband MSAs:** Parametric Study of RMSAs, Orthogonal Feeds	7

for Dual Polarization, Circularly Polarized RMSA, Broadband Suspended RMSA, Broadband Thick RMSA with Various Probes, Frequency and Impedance Scaling of RMSA, Resonance Frequency, Input Impedance and Voltage Distribution, Radiation Pattern, Broadband CMSAs, Circularly Polarized CMSAs	
Unit III Planar Multi resonator Broadband MSAs: Introduction, Mechanism of Parasitic Coupling for Broad BW, Gap-Coupled RMSAs, Radiating-Edge Gap-Coupled RMSAs, Non radiating-Edge Gap-Coupled RMSAs, Broadband Microstrip Antennas, Four-Edge Gap-Coupled RMSAs, Design Guidelines for Gap-Coupled RMSAs, Other Gap-Coupled Multi resonator RMSAs, Directly Coupled RMSAs, Radiating-Edge, Non radiating-Edge Directly Coupled RMSAs Four-Edge Directly Coupled RMSAs	7
Unit IV **Multilayer Broadband MSAs** : Electromagnetically Coupled MSAs, Microstrip Line Feed ECMSAs, Parametric Study of Coaxial-Fed Square ECMSAs, Coaxial-Fed Stacked CMSAs, Coaxial-Fed Stacked ETMSAs, Design Example Using Stacked-Square MSA on Air Substrate, ACMSAs, Parametric Study of ACMSAs, Effect of the Shape of the Coupling Aperture, Stacked ACMSAs, Resonant Slot ACMSAs.	7
Unit V **Stacked Multi resonator MSAs, Stacked** Multi resonator Rectangular Patches on Thick Substrates, Three Rectangular Patches at the Bottom and One Patch on the Top, One Rectangular Patch at the Bottom and Three Patches on the Top, Three Rectangular Patches at the Bottom and Three Patches on the Top. **Compact Broadband MSAs:** Compact Shorted RMSAs, Partially Shorted RMSAs, Effect of Dimensions of RMSAs with a Single Shorting Post, Effect of the Position of the Single Shorting Post.	7
Unit VI **Tunable and Dual-Band MSAs:** Tunable MSAs, Stub-Loaded Tunable MSAs, Tunable MSAs Using Shorting Posts, Tunable MSAs Using Varactor Diodes, Optically Tuned MSA. **Broadband Circularly Polarized MSAs:** Linear, Circular, and Elliptical Polarizations. Dual-Feed Circularly Polarized MSAs, Square MSA with Two Feeds.	7
Suggested list of Tutorials and Assignments: As suggested by the course teacher	
Suggested Text Books:	
1.	Broadband Microstrip Antennas by Girish Kumar, K. P. Ray
Suggested Reference Books:	
1.	

Course Outcome and Program Outcome Mapping

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10
CO 1	1	1	1	1	1	1	1	1		

CO 2	1	1	1	1	1	1	1	1		
CO 3	1	1	1	1	1	1	1	1		
CO 4	1	1	1	1	1	1	1	1		
CO 5										
CO6										

Level of Mapping as: Low 1, Moderate 2, High 3

Class, Part & Semester	**:**	**First Year M. Tech (E&TC), Part I, Sem-I**					
Course Title	**:**	**Computational Electromagnetics (Elective-I)**			***Course Code*:**	**:**	METCE13
Teaching Scheme (Hours)	**:**	Lecture :	3 Hrs/week		***Total Credits***	**:**	3
		Tutorial :	-- Hrs/week				
Evaluation Scheme (Marks)	**:**	ISE=40	ESE = 60	Grand Total=100	***Duration of ESE***	**:**	3 hrs
Revision:	**:**	Fourth			***Month***	**:**	July 2025
Pre-requisites *(if any)*	**:**	Electromagnetic fields					
Course Domain	**:**	Communication					

Course Rationale: This course on Computational Electromagnetics is targetted at senior undergraduate students and beginning graduate students who have taken a first course in Engineering Electromagnetics. The course covers the mathematical formulation of the main methods currently in use by the community, namely: Integral Equations Methods (and their solution by the Method of Moments), the Finite Element Method, and the Finite Difference Time Domain method. These methods are illustrated by their use in solving scattering problems and antenna radiation/impedance calculation problems. Additional topics include introduction to inverse problems, calculating the mutual coupling between antennas, finding the electromagnetic modes of a waveguide, and techniques to hybridize the Finite Element Method with the Integral Equation Method. Programming issues faced in the implementation of these methods will also be highlighted.

Course Objectives: The Course teacher will		***Course Outcomes:*** Students will be able to	
32.	Explain Surface integral equations in 2D, Green's functions	**32.**	**Understand** Surface integral equations in 2D, Green's functions
33.	Solve volume integral equations by method of moments, Introduce finite	**33.**	Solve volume integral equations by method of moments, Introduce finite

	element methods, Finite element method in 1D		element methods, Finite element method in 1D
34.	Introduce Finite difference time domain method	**34.**	solve problems based on Finite difference time domain method
35.	Teach Applications of CEM for antenna radiation problems and hybrid methods	**35.**	Understand Applications of CEM -- antenna radiation problems and hybrid methods
36.		**36.**	

Curriculum Content	**Hours**
Unit I Review of vector calculus, electromagnetic fields, and an overview of computational electromagnetics, Numerical integration, Introduction to integral equations, and the Helmholtz equation	6
Unit II Surface integral equations in 2D, Green's functions , Solving surface integral equations by method of moments	7
Unit III Solving volume integral equations by method of moments, Introduction to finite element methods, Finite element method in 1D	7
Unit IV Finite element method in 2D, Finite difference time domain method - introduction	7
Unit V Finite difference time domain method - materials and boundary conditions , Finite difference time domain method - perfectly matched layers	7
Unit VI Applications of CEM -- inverse problems and antenna radiation problems , Applications of CEM -- antenna radiation problems and hybrid methods	7
Suggested list of Tutorials and Assignments: As suggested by the course teacher	
Suggested Text Books:	
1. Computational Electromagnetics by Prof. Uday Khankhoje	
2.	
Suggested Reference Books:	

1.	

Course Outcome and Program Outcome Mapping

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10
CO 1	1	1	1	1	1	1	1	1		
CO 2	1	1	1	1	1	1	1	1		
CO 3	1	1	1	1	1	1	1	1		
CO 4	1	1	1	1	1	1	1	1		
CO 5										
CO6										

Level of Mapping as: Low 1, Moderate 2, High 3

Elective -II

Class, Part & Semester	**:**	**First Year M. Tech (E&TC), Part I, Sem-I**					
Course Title	**:**	**Advanced Communication System (Elective-II)**			***Course Code*:**	**:**	METCOE11
Teaching Scheme (Hours)	**:**	Lecture :	3 Hrs/week		***Total Credits***	**:**	3
		Tutorial :	-- Hrs/week				
Evaluation Scheme (Marks)	**:**	ISE=40	ESE = 60	Grand Total=100	***Duration of ESE***	**:**	3 hrs
Revision:	**:**	Fourth			***Month***	**:**	July 2025
Pre-requisites *(if any)*	**:**	Analog and Digital Communication					
Course Domain	**:**	Communication					

Course Rationale*:* Advanced Communication refers to the utilization of sophisticated technologies to enable seamless connectivity and interaction between various devices and systems, leading towards a more interconnected global community.

Course Objectives: The Course teacher will	*Course Outcomes:* Students will be able to

37.	Provide understanding of advanced concepts of data communication.	37.	Understand the concepts and technologies used in the data communication domain.
38.	Along with basics it also covers the protocols like USART, USB, I2C , CAN etc.	38.	Understand the various protocols used in the various data communication applications.
39.	Provide student with theoretical background and applied knowledge so that they can design an optimum Single and multi-carrier communication system under given power, spectral and error performance constraints.	39.	Get knowledge about latest trends in the data communication field
40.	Analyze the error performance of digital modulation techniques.	40.	Analyze the design parameters of a single and multi-carrier communication system.
41.		41.	Use mathematical tools to analyze the performance of communication systems.
42.		42.	Use probability theory and stochastic processes in communication system applications.

Curriculum Content	**Hours**
Unit I Digital Modulation Schemes: BPSK, QPSK, 8PSK, 16PSK, 8QAM, 16QAM, DPSK – Methods, Bandwidth Efficiency, Carrier Recovery, Clock Recovery.	6
Unit II Multiplexing: Frequency Division Multiplexing (FDM), Time Division Multiplexing (TDM), Multiplexing Application, SMDS Switching: Circuit Switching, Packet Switching, Message Switching. Networking and Interfacing Devices: Repeaters, Bridges, Routers, Gateway, Other Devices.	7
Unit III Basic Concepts of Data Communications, Interfaces and Modems: Data Communication Networks, Protocols and Standards, CAN, UART, USB, I2C, I2S, Line Configuration, Topology, Transmission Modes, Digital Data Transmission, DTE-DCE interface, Categories of Networks – TCP/IP Protocol suite and Comparison with OSI model.	7
Unit IV Error Correction: Types of Errors, Vertical Redundancy Check (VRC), LRC, CRC, Checksum, Error Correction using Hamming code Data Link Control: Line Discipline, Flow Control, Error Control Data Link Protocols: Asynchronous Protocols, Synchronous Protocols, Character Oriented Protocols, Bit-Oriented Protocol, Link Access Procedures.	7
Unit V Random Access, Aloha- Carrier Sense Multiple Access (CSMA)- Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA), Controlled Access- Reservation Polling-Token Passing.	6

Unit VI Channelization, Frequency- Division Multiple Access (FDMA), Time - Division Multiple Access (TDMA), Code - Division Multiple Access (CDMA), Orthogonal Frequency-Division Multiplexing (OFDM) and Orthogonal Frequency-Division Multiple Access (OFDMA).	7

Suggested list of Tutorials and Assignments: As suggested by the course teacher

Suggested Text Books:	
1.	Data Communication and Computer Networking - B. A.Forouzan, 2nd Ed., 2003, TMH.
2.	Advanced Electronic Communication Systems - W. Tomasi, 5th Ed., 2008, PEI
3.	
Suggested Reference Books:	
1.	Data and Computer Communications - William Stallings, 8th Ed., 2007, PHI.
2.	Data Communication and TeleProcessing Systems -T. Housely, 2nd Ed, 2008, BSP.
3.	Data Communications and Computer Networks- Brijendra Singh, 2nd Ed., 2005, PHI.
4.	Computer Networks; By: Tanenbaum, Andrew S; Pearson Education Pte. Ltd., Delhi, 4th Edition
5.	Manufacturers Device data sheets

Course Outcome and Program Outcome Mapping

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10
CO 1		2	2							
CO 2		3							2	
CO 3				2						2
CO 4	2					3				3
CO 5		2	2						3	
CO6		2	2			2				

Level of Mapping as: Low 1, Moderate 2, High 3

Class, Part & Semester	**:**	**First Year M. Tech (E&TC), Part I, Sem-I**					
Course Title	**:**	**Reconfigurable Computing (Elective-II)**			***Course Code*:**	**:**	METCOE12
Teaching Scheme (Hours)	**:**	Lecture :	3 Hrs/week		***Total Credits***	**:**	3
		Tutorial :	-- Hrs/week				
Evaluation Scheme (Marks)	**:**	ISE=40	ESE = 60	Grand Total=100	***Duration of ESE***	**:**	3 hrs
Revision:	**:**	Fourth			***Month***	**:**	July 2025

Pre-requisites *(if any)*	**:**	FPGA Basics
Course Domain	**:**	**Design and Computing**

Course Rationale: Reconfigurable (adaptive) computing is a novel yet important research field investigating the capability of hardware to adapt to changing computational requirements such as emerging standards, late design changes, and even to changing processing requirements arising at run-time. Reconfigurable computing thus benefits from a) the programmability of software similar to the Von Neumann computer and b) the speed and efficiency of parallel hardware execution.

Course Objectives: The Course teacher will able to		***Course Outcomes:*** Students will be able to	
43.	Make students to understand various computing architectures	**43.**	Understand the concept of reconfigurable computing and its integration on computing platforms.
44.	Provide students the concept of handling issues of reconfigure computing	**44.**	Design, implement and analyze reconfigurable systems in the recent application domains using HDL.
45.	Provide students implementation approaches of FPGA design in view of reconfiguration	**45.**	Use advanced EDA tools to simulate and synthesize HDL codes for reconfigurable architectures.
46.		**46.**	get familiar with the possibilities and rapidly growing interest in adaptive hardware and corresponding design techniques
47.		**47.**	Analyze the existing Reconfigurable Processing Fabric (RPF) Architectures
48.		**48.**	

Curriculum Content	**Hours**
Unit I Domain of RC: General Purpose Computing, Domain-Specific Processors, Application-Specific Processors, Reconfigurable Computing, Fields of Application. Architecture of Field Programmable Gate Arrays	6
Unit II Reconfigurable Processing Fabric (RPF) Architectures: Fine grained, Coarse-Grained, Integration of RPF into Traditional Computing Systems. Early systems of Reconfigurable computing: PAM, VCC, Splash, PRISM, Teramac, Cray, SRC, non-FPGA research, other issues.	7
Unit III Contexts, Context switching; Area calculations for PE Efficiency, ISP, Hot Reconfiguration; Case study. Architectures for existing multi FPGA systems, Arrays for fast computations, CPLDs, FPGAs, Multi context, Partial Reconfigurable Devices; TSFPGA, DPGA, Mattrix;	7

Best suitable approach for RD; Case study Reconfiguration Management: Reconfiguration, Configuration architectures, managing reconfiguration process, reducing reconfiguration time, configuration security.	
Unit IV RC Applications: Implementing applications with FPGAs, various applications and use of reconfiguration: Video Streaming, , Distributed arithmetic, Adaptive Controller, Adaptive cryptographic systems, Software Defined Radio, High-Performance Computing, Automatic target recognition systems.	7
Unit V Implementation: Integration, FPGA Design Flow, System On A Programmable Chip: Introduction to SoPC, Adaptive Multiprocessing on Chip. Reconfiguration Project Design Approaches: J-Bit, Modular, Early Access, Vivad.	7
Unit VI Software challenges in System on chip; Testability challenges; Case studies. Modeling, Temporal partitioning algorithms, Online temporal placement, Device space management.	6

Suggested list of Tutorials and Assignments: As suggested by the course teacher

Suggested Text Books:	
1.	Wolf Wayne, FPGA Based System Design, Pearson Edu, 2004.
2.	Hauck Scott, Dehon A, "Reconfigurable Computing: The Theory and Practice of FPGA- Based Computation", Elsevier.
3.	
Suggested Reference Books:	
1.	Vivado Partial Reconfiguration.pdf: user guide 909 by Xilinx Revision: 04/06/2016
2.	Maya Gokhale, Paul Ghaham, "Reconfigurable Computing", Springer Publication.
3.	Bobda Christophe, "Introduction to Reconfigurable Computing: Architectures, Algorithms, and Applications", Springer.
4.	

Course Outcome and Program Outcome Mapping

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10
CO 1		3	3	2						
CO 2	3					2				
CO 3				2						
CO 4			2							
CO 5	3				2					
CO6										

Level of Mapping as: Low 1, Moderate 2, High 3

Class, Part & Semester	**:**	**First Year M. Tech (E&TC), Part I, Sem-I**				
Course Title	**:**	**VLSI Testing & Testability (Elective -II)**		***Course Code*:**	**:**	METCOE13
Teaching Scheme (Hours)	**:**	Lecture : 3 Hrs/week Tutorial : -- Hrs/week		***Total Credits***	**:**	3
Evaluation Scheme (Marks)	**:**	ISE=40	ESE = 60	***Duration of ESE***	**:**	3 hrs
Revision:	**:**	Fourth		***Month***	**:**	July 2025
Pre-requisites *(if any)*	**:**	Basic knowledge in the following areas: digital design, optimization algorithms, and computer architecture.				
Course Domain	**:**	**VLSI**				

Course Rationale: VLSI testing verifies the functionality and detects defects in integrated circuits, while testability focuses on making designs easier to test, improving efficiency and reducing costs.

Course Objectives: The Course teacher will		***Course Outcomes:*** Students will be able to	
49.	Introduce design process in VLSI	49.	Accept challenges in VLSI Testing at different abstraction levels
50.	Teach the logical and Fault simulation models	50.	Understand fault models for generation of test vectors
51.	Make students to learn techniques for design of testability	51.	Calculate observability and controllability parameters of circuit
52.	Make students to study hardware and software verification issues for testing	52.	Enhance testability of a circuit. Use simulation techniques for designing and testing of VLSI circuits
53.		53.	
54.		**54.**	

Curriculum Content	**Hours**
Unit I Introduction to the concepts and techniques of VLSI (Very Large Scale Integration) design verification and testing, VLSI testing process and test equipment, test economics and product quality	7
Unit II Fault modeling, testing and verification in VLSI design process, test methods, logic and fault simulation, modeling circuits for simulation, algorithms for true- value simulation and algorithms for fault simulation.	7

Unit III Statistical methods for fault simulation, testability measures, combinational circuit test generation, sequential circuit test generation, memory test.	6
Unit IV Fault Simulation Application and Methods: Fault Simulation, Fault Simulation Applications, Fault Simulation Technologies. Test pattern Generation Methods and Algorithm: Test Generation Basics, Controllability and Observability, Random Test Generation.	6
Unit V Design for testability, Scan and Boundary scan architectures, Built-in Self-test (BIST) and current-based testing, analog test bus standard, System test and core-based design, ATPG, Embedded core test fundamentals.	7
Unit VI Design verification techniques based on simulation, analytical and formal approaches. Functional verification. Timing verification. Formal verification. Basics of equivalence checking and model checking. Hardware emulation.	7
Suggested list of Tutorials and Assignments: As suggested by the course teacher	

Suggested Text Books:	
1.	Bushnell M L, Agrawal V D, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers.
2.	Abramovici M, Breuer M A and FriedmanA D, "Digital systems and Testable Design", JaicoPublications.
3.	
Suggested Reference Books:	
1.	Crouch A L, "Design Test for Digital IC's and Embedded Core Systems", Prentice Hall.
2.	Kropf T, "Introduction to Formal Hardware Verification," Springer Publications
3.	Niraj K. Jha, Sandeep Gupta, Testing of Digital Systems, 1st edition, Cambridge University Press, 2003. ISBN: 0521-77356-3
4.	M. Abramovici, M. A. Breuer and A. D. Figriieta, Digital Systems Testing and Testable Design, Wiley-IEEE Press, 1994, ISBN: 978-0-7803-1062-9.
5.	
6.	

Course Outcome and Program Outcome Mapping

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10
CO 1		3			2	2				
CO 2			3	2					1	

CO 3				2		3				
CO 4	2	3	2						2	
CO 5										
CO6										

Level of Mapping as: Low 1, Moderate 2, High 3

Class, Part & Semester	:	**First Year M. Tech (E&TC), Part I, Sem-I**					
Course Title	:	**Seminar-I**			***Course Code*:**	:	METCC 14
Teaching Scheme (Hours)	:	Practical :	2 Hrs/week		***Total Credits***	:	1
Evaluation Scheme (Marks)	:	/IOE= 50 Marks	EOE= ---	Total= 50 marks	***Duration of EPE***	:	----
Revision:	:	Fourth			***Month***	:	July 2025
Pre-requisites *(if any)*	:	**Advance Technology Studies**					
Course Domain	:	**Technology Exchange**					

Course Rationale: Students should get acquainted with the advance topics in the field of Electronic, IT , E&TC and Computer Engineering

Course Objectives: The Course teacher will		***Course Outcomes:*** Students will be able to	
1.	*To encourage students for research development*	1	*Demonstrate and explore New Technology*
2.		2	*Inculcate ability to make presentation*
3.		3.	*Explore the research*
4.		4	*Inculcate innovations*
5			
6.			

Course Outcome and Program Outcome Mapping

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10

CO 1					3				3	
CO 2	3						2			
CO 3				2	2				2	
CO 4		3	3			2				2
CO 5										
CO6										

Level of Mapping as: Low 1, Moderate 2, High 3

Class, Part & Semester	:	**First Year M. Tech (E&TC), Part I, Sem-I**							
Course Title	:	**Lab-1: Advance Computer Networks**			***Course Code*:**	:	METCC15		
Teaching Scheme (Hours)	:	Practical :	2 Hrs/week		***Total Credits***	:	1		
Evaluation Scheme (Marks)	:	IOE=50 marks	EOE= -----	Total=50	***Duration of EPE***	:	----		
Revision:	:	Fourth			***Month***	:	July 2025		
Pre-requisites *(if any)*	:	Computer networking theory knowledge							
Course Domain	:	**Communication**							
Course Rationale:									

Course Objectives: The Course teacher will		***Course Outcomes:*** Students will be able to			
1.	This Lab course will provide in depth knowledge about networking concepts and students will be familiar with all various protocols.	1.	Identify the different types of network devices and their functions within a network.		
2.		2.	Understand and build the skills of sub-netting and routing mechanisms.		
3.		3.	Understand basic protocols of computer networks, and how they can be used to assist		

			in network design and implementation		
4.		**4.**			
List of Experiments					
Sr. No.	**Experiments**				
1.	Study of Networking Commands (Ping, Tracert, TELNET, ns lookup, net stat, ARP, RARP) and Network Configuration Files....				
2.	Linux Network Configuration. a. Configuring NIC's IP Address. b. Determining IP Address and MAC Address using if-config command. c. Changing IP Address using if-config. d. Static IP Address and Configuration by Editing. e. Determining IP Address using DHCP. f. Configuring Hostname in /etc/hosts file				
3.	Design TCP iterative Client and Server application to reverse the given input sentence.				
4.	Design a TCP concurrent Server to convert a given text into upper case using multiplexing system call "select".				
5.	Design UDP Client Server to transfer a file				
6.	Configure a DHCP Server to serve contiguous IP addresses to a pool of four IP devices with a default gateway and a default DNS address. Integrate the DHCP server with a BOOTP demon to automatically serve Windows and Linux OS Binaries based on client MAC address. a. Configure DNS: Make a caching DNS client, and a DNS Proxy; implement reverse DNS and forward DNS, using TCP dump/Wireshark characterise traffic when the DNS server is up and when it is down.				
7.	Configure a mail server for IMAP/POP protocols and write a simple SMTP client in C/C++/Java client to send and receive mails.				
8.	Configure FTP Server on a Linux/Windows machine using a FTP client/SFTP client characterise file transfer rate for a cluster of small files 100k each and a video file of 700mb.Use a TFTP client and repeat the experiment.				
9.	Signaling and QoS of labeled paths using RSVP in MPLS				
10.	Find shortest paths through provider network for RSVP and BGP.				
11.	Understand configuration, forwarding tables, and debugging of MPLS				
12.					
General Instructions: if any regarding course delivery and assessment					
Suggested Text Books/ Reference Books/Manual					
1.	Wireless Communication System -Abhishek yadav –University Sciences Press, 2009.				
2.	Andrew .S. Tanenbaum, "Computer Networks", 4th Edition, Prentice Hall of India, New Delhi, 2008. .				
3.	High Performance TCP-IP Networking -Mahaboob Hassan -Jain Raj-PHI.				
4.	Fred Halsall, "Data Communications and Networking", 5th Edition, McGraw Hill, 2012.				

Course Outcome and Program Outcome Mapping

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10
CO 1		2								
CO 2		3	3		3		1			2
CO 3				2					1	

Level of Mapping as: Low 1, Moderate 2, High 3

Class, Part & Semester	**:**	**First Year M. Tech (E&TC), Part I, Sem-I**					
Course Title	**:**	**Lab-2: Microwave Theory and Circuits**			***Course Code*:**	**:**	METCC-16
Teaching Scheme (Hours)	**:**	Practical :	2 Hrs/week		***Total Credits***	**:**	-1
Evaluation Scheme (Marks)	**:**	IOE= 50 Marks	EOE= ----	Total= 50 marks	***Duration of EPE***	**:**	----
Revision:	**:**	Fourth			***Month***	**:**	July 2026
Pre-requisites	**:**	Microwave Engineering					

(if any)		
Course Domain	**:**	Communication

Course Rationale: Please write it in 3 to 4 lines

Course Objectives: The Course teacher will		***Course Outcomes:*** Students will be able to	
1.	*Impart in depth knowledge about various devices and the measurements*	1.	*understand gunn diode characteristics and attenuation measurements*
2.	*Impart in depth knowledge about directional coupler*	2.	*measure various parameters of Directional coupler*
3.	*Impart in depth knowledge about* VSWR measurement	3.	*Measure VSWR*
4.	*Impart in depth knowledge about Impedance and frequency measurement*	4.	*Measure Impedance and frequency*
5	*Impart in depth knowledge about waveguide parameters measurement*	5.	*Measure waveguide parameters*
6.	*Impart in depth knowledge about scattering parameters*	6.	*Measure scattering parameters of circulator and magic TEE*

List of Experiments

Sr. No.	**Experiments**
1.	GUNN DIODE CHARACTERISTICS
2.	ATTENUATION MEASUREMENT
3.	DIRECTIONAL COUPLER CHARACTERISTICS
4.	VSWR MEASUREMENT
5.	IMPEDANCE AND FREQUENCY MEASUREMENT
6.	WAVEGUIDE PARAMETERS MEASUREMENT
7.	SCATTERING PARAMETERS OF CIRCULATOR
8.	SCATTERING PARAMETERS OF MAGIC TEE
9.	
10.	
11.	
12.	

General Instructions: if any regarding course delivery and assessment

Suggested Text Books/ Reference Books/Manual

1.	Microwave theory and techniques by Prof Girish Kumar
2.	
3.	
4.	

Course Outcome and Program Outcome Mapping

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10
CO 1	2	1	1	1	1	1	1	1		
CO 2	2	1	1	1	1	1	1	1		
CO 3	1	1	1	1	1	1	1	1		
CO 4	2	1	1	1	1	1	1	1		
CO 5	1	1	1	1	1	1	1	1		
CO6	1	1	1	1	1	1	1	1		

Level of Mapping as: Low 1, Moderate 2, High 3

Semester-II

Class, Part & Semester	**:**	**First Year M. Tech (E&TC), Part I, Sem-II**					
Course Title	**:**	**Intellectual Property Rights**			***Course Code*:**	**:**	METCAC2
Teaching Scheme (Hours)	**:**	Lecture :	2 Hrs/week		***Total Credits***	**:**	2
		Tutorial :	-- Hrs/week				
Evaluation Scheme (Marks)	**:**	ISE=)nil	IOE = 50	Grand Total=50	***Duration of ESE***	**:**	—-
Revision:	**:**	Fourth			***Month***	**:**	July 2025
Pre-requisites *(if any)*	**:**	Basic Legal Awareness, Digital Literacy					
Course Domain	**:**	Audit Course					

Course Rationale: The course on Intellectual Property Rights (IPR) is designed to provide students with an in-depth understanding of the importance of intellectual property in fostering innovation, creativity, and economic development. As the global economy becomes increasingly knowledge-driven, protecting and managing intellectual property is critical for individuals, organizations, and nations.

Course Objectives: The Course teacher will		***Course Outcomes:*** Students will be able to	
55.	Provide a comprehensive understanding of the concept, origin, and types of Intellectual Property Rights (IPR) and their significance in the global context.	55.	Explain the fundamental concepts, origin, and significance of various types of Intellectual Property Rights (IPRs) in protecting innovations and creations.
56.	Introduce the legal framework of IPR, including the TRIPS agreement and its relationship with the WTO	56.	Apply the knowledge of patent laws, registration procedures, and infringement remedies in the protection of inventions and technologies
57.	Familiarize students with the processes and laws related to patents, copyrights, and trademarks, along with their infringements and remedies	57.	Demonstrate an understanding of copyright laws, including software copyrights, piracy issues, and the remedies for infringement.
58.	Understand the significance of designs, geographical indications, and layout designs, as well as their protection under international and national laws.	58.	Analyze and manage issues related to trademarks, including registration, infringement, and offenses in cyberspace, such as domain name disputes.
59.	Explore the legal provisions and ethical considerations related to the Information Technology Act, 2000, including cybercrime, e-commerce, and digital signatures.	59.	Evaluate the legal framework for design protection, including the Semiconductor Integrated Circuits Layout Design Act and international conventions.

60.	Develop the ability to identify, register, and manage intellectual property rights in various domains, including traditional knowledge and modern technologies.	60.	Assess the implications of the Information Technology Act, 2000, particularly in the areas of e-governance, e-commerce, digital signatures, and combating cybercrime.

Curriculum Content	**Hours**
Unit I Introduction to IPR: Meaning of property, Origin, Nature, Meaning of Intellectual Property Rights, Introduction to TRIPS and WTO, Kinds of Intellectual property rights—Copy Right, Patent, Trade Mark, Trade; Secret and trade dress, Design, Layout Design, Geographical Indication, Plant. Varieties and Traditional Knowledge	5
Unit II Patent Rights and Copy Rights— Origin, Meaning of Patent, Types, Inventions which are not patentable, Registration Procedure, Rights and Duties of Patentee, Assignment and license, Restoration of lapsed Patents, Surrender and Revocation of Patents, Infringement, Remedies & Penalties	5
Unit III Copy Right—Origin, Definition &Types of Copy Right, Registration procedure, Assignment & license, Terms of Copy Right, Piracy, Infringement, Remedies, Copy rights with special reference to software	4
Unit IV Trade Marks: Origin, Meaning & Nature of Trade Marks, Types, Registration of Trade Marks, Infringement & Remedies, Offences relating to Trade Marks, Passing Off, Penalties. Domain Names on cyber space	4
Unit V Design- Meaning, Definition, Object, Registration of Design, Cancellation of Registration, International convention on design, functions of Design. Semiconductor Integrated circuits and layout design Act-2000**.**	4
Unit VI Basic Tenents Of Information Technology Act-2000, IT Act - Introduction, E-Commerce and legal provisions, E- Governance and legal provisions, Digital signature and Electronic Signature. Cybercrimes.	5
Suggested list of Tutorials and Assignments: As suggested by the course teacher	

Suggested Text Books/Reference Books	
1.	Intellectual Property Rights and the Law, Gogia Law Agency, by Dr. G.B. Reddy
2.	Law relating to Intellectual Property, Universal Law Publishing Co, by Dr. B.L.Wadehra
3.	**IPR by P. Narayanan**
Suggested :	

1.	Law of Intellectual Property, Asian Law House, Dr. S. R. Myneni.
2.	
3.	
4.	
5.	
6.	

Course Outcome and Program Outcome Mapping

Level of Mapping as: Low 1, Moderate 2, High 3

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10
CO 1			2					2		
CO 2			3				3	2	3	
CO 3			3				2			
CO 4						3	2			
CO 5						3	2			
CO6			3				2	2		

Class, Part & Semester	**:**	**First Year M. Tech (E&TC), Part I, Sem-II**					
Course Title	**:**	**Real Time Operating System**			***Course Code*:**	**:**	METCC21
Teaching Scheme (Hours)	**:**	Lecture :	3 Hrs/week		***Total Credits***	**:**	3
		Tutorial :	-- Hrs/week				
Evaluation Scheme (Marks)	**:**	ISE=40	ESE = 60	Grand Total=100	***Duration of ESE***	**:**	3 hrs
Revision:	**:**	Fourth			***Month***	**:**	July 2025
Pre-requisites *(if any)*	**:**	Knowledge of operating system					
Course Domain	**:**	**Embedded**					

Course Rationale: This course is to introduce students with the basic concepts and approaches in the design and analysis of real-time operating systems. It covers design considerations of real time operating systems, task scheduling, threads, multitasking, task communication and synchronization. Applications of the course include real time operating systems in image processing, fault tolerant applications and control systems.

Course Objectives: The Course teacher will	***Course Outcomes:*** Students will be able to

61.	Explain the concepts of operating systems and principles of real time operating systems, implementation aspects of real time concepts in embedded systems.	**61.**	Recall real time operating system to provide resource management and synchronization for communication systems.
62.	Teach the design of real time operating system by using the concepts of Timers, I/O subsystem and Memory management units.	**62.**	Compare soft real-time operating system and hard real-time operating systems for the priority-based task scheduling.
63.	Explain software development process and tools like Vxworks and mu COS for real time operating system applications.	**63.**	Outline the components of real time operating systems for the design of reliable embedded system.
64.		**64.**	Analyze finite state machine for the task scheduling and execution in kernel models.
65.		**65.**	Develop a semaphore token for the execution of one or more threads in mutual exclusion.
66.		**66.**	Interpret message queue in asynchronous communications protocol for send and receive messages simultaneously.

Curriculum Content	**Hours**
Unit I **REAL TIME OPERATING SYSTEM PRINCIPLES** History of operating systems, defining RTOS, classification of real-time systems, the scheduler, objects, services and key characteristics of RTOS, Tasks: Defining a task, task states and scheduling, typical task operations, typical task structure. Semaphores: Defining semaphores, typical semaphore operations, typical semaphore use; Message Queues Defining message queues, message queue states, message queue content, message queue storage, typical message queue operations; typical message queue use other kernel objects: Pipes, event registers, signals, condition variables.	08
Unit II **RTOS DESIGN CONSIDERATIONS** Timer and Timer Services: Real-time clocks and system clocks, programmable interval timers, timer interrupt service routines, model for implementing the soft-timer handling facility, timing wheels. I/O subsystem: Basic I/O concepts, the I/O sub system; Memory management: Dynamic memory allocation, fixed size memory management, blocking vs. Non-blocking memory functions, hardware memory management units	07
Unit III **TASKS COMMUNICATION AND SYNCHRONIZATION** Synchronization and Communication: Synchronization, communication, resource synchronization methods, common practical design patterns; common design problems: Resource classification, deadlocks, priority inversion.	06

Unit IV Real Time Operating Systems (μC/OS):Real-Time Software Concepts, Kernel Structure, Task Management, Time Management, Inter task Communication & Synchronization, Memory Management, and Porting μCos-II.	07
Unit V Linux/RT Linux: Features of Linux, Linux commands, File Manipulations, Directory, Pipes and Filters, File Protections, Shell Programming, System Programming, RT Linux Modules, POSIX Threads, Mutex Management, Semaphore Management.	06
Unit VI **RTOS APPLICATION DOMAINS (09) :**Comparison and study of RTOS: Vx works and COS, Case studies: RTOS for image processing, embedded RTOS for voice over IP, RTOS for fault tolerant applications, RTOS for control systems	06

Suggested list of Tutorials and Assignments: As suggested by the course teacher	
Suggested Text Books:	
1.	Labrossy J. J, Lawrence, "μC/OS-II, The real time Kernel", R & D Publication.
2.	2. Dr Prasad K V K K, "Embedded Real Time Systems: Concepts, Design & Programming", Dreamtech Publication.
3.	**Simon D. E, "An Embedded Software Primer", Pearson education.**
Suggested Reference Books:	
1.	Tanenbaum A S, "Modern Operating Systems", Prentice Hall.
2.	Raj Kamal, "Embedded Systems Architecture, Programming and design", Tata McGraw-Hill
3.	

Course Outcome and Program Outcome Mapping

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10
CO 1		3								
CO 2		3	2							
CO 3				2						
CO 4	2		2			2				
CO 5		2								

CO6			2			2				

Level of Mapping as: Low 1, Moderate 2, High 3

Class, Part & Semester	**:**	**First Year M. Tech (E&TC), Part I, Sem-I**					
Course Title	**:**	**Advanced Embedded System**			***Course Code*:**	**:**	METCC22
Teaching Scheme (Hours)	**:**	Lecture :	3 Hrs/week		***Total Credits***	**:**	3
		Tutorial :	__ Hr/week				
Evaluation Scheme (Marks)	**:**	ISE=40	ESE = 60	Grand Total=100	***Duration of ESE***	**:**	3 hrs
Revision:	**:**	Fourth			***Month***	**:**	July 2025
Pre-requisites *(if any)*	**:**	**Embedded System**					
Course Domain	**:**	**Integrated Circuits**					

Course Rationale: An advanced embedded systems course is designed to build upon foundational knowledge, equipping students with in-depth skills in hardware and software, real-time operating systems, and advanced programming techniques, preparing them for specialized roles in the industry.

Course Objectives: The Course teacher will		***Course Outcomes:*** Students will be able to	
67.	Teach to make understand basic concepts of Embedded Systems.	67.	Understand and explain the concepts of Embedded Systems and apply the knowledge of Computer Architecture in building Embedded Systems.
68.	Teach to make the stude aware know development of Hardware Software co-design in Embedded System.	68.	Analyze the real-time deterministic response of embedded systems and various peripherals involved in Embedded system
69.	To understand Architecture of ARM-32 bit Microcontroller.	69.	Design low power, real time deterministic Embedded Systems and Develop C programs, execute & demonstrate on embedded target boards like Raspberry Pi, Arduino, etc.

70.	To analyse Instruction sets by Assembly basics, Instruction list and description.	70.	Perform in a team to design and develop useful embedded systems and make an effective oral presentation on topics allocated by instructor pertaining to Computer Architecture, Embedded Systems, Analog and Digital peripherals.
71.		**71.**	
72.		**72.**	

Curriculum Content	**Hours**
Unit I Introduction to Embedded Systems, Real time nature of ES, Architectures of ES including multi core architecture, Graphic Processing Units(GPU), Typical Embedded System: Core of the Embedded System, Memory, Sensors and Actuators, Communication Interface, Embedded Firmware, Other System Components. Case Study Raspberry Pi 3.	7
Unit II Characteristics and Quality Attributes of Embedded Systems: Hardware Software Co Design and Program Modeling: Fundamental Issues in Hardware Software Co-Design, Computational Models in Embedded Design, Introduction to Unified Modeling Language, Hardware Software Trade-offs. Embedded Firmware Design and Development: Embedded Firmware Design Approaches, Embedded Firmware Development Languages(C, C++, Python, VHDL/Verilog).	7
Unit III Introduction to SoC: Case Study Xilinx Zynq, Anatomy, Design Reuse, Abstraction, SoC Design Flow, Zynq APU, ARM Model, Logic Fabric, Block RAM, GPIO, Communication Interfaces, ZynqSoc Design Overview.	6
Unit IV Device Comparison: Device Selection Criteria, Zynqvs FPGA, Zynqvs Standard Processor, Zynqvs Dicrete FPGA Processor, Zynq Architecture and Design Flow, Embedded Systems and FPGA, Processors and Buses.	7
Unit V USB Basics: Uses and limits, Benefits, Evolution, Bus components, Division of labor, Transfer basics, Elements of a transfer, USB 2.0 transactions, Ensuring successful transfers, Control transfers, Bulk transfers, Interrupt transfers, Isochronous transfers, Enumeration: Process and Descriptors.	6
Unit VI Hosts for Embedded Systems: Targeted Host, Targeted Peripheral List, Targeted Host types, Bus current, turning off bus power, Embedded Hosts, Differences from conventional host ports, Functioning as a USB device, OTG devices, A-Device and B-	7

Device, OTG descriptor, Host Negotiation Protocol, Role Swap Protocol		
Suggested list of Tutorials and Assignments: As suggested by the course teacher		
Suggested Text Books:		
1.	James K. Peckol , "Embedded systems - A contemporary design tool", John Wiley, 2008	
2.	"Embedded System Design A unified Hardware/Software Introduction" Frank Vahid/ Tony Givargis, John Wiley & Sons Pte Ltd.	
3.		
Suggested Reference Books:		
1.	Hennessy and Patterson, Computer Architecture: A Quantitative Approach", Latest Edition	
2.	2. Shibu K V, "Introduction to Embedded Systems", Tata McGraw Hill Education Private Limited, 2009	
3.	3. The Zynq Book, by Crockett, Elliot, Enderwitz& Stewart, University of Strathclyde Glasgow, 2014	
4.	4. USB Complete: The Developer's Guide, Jan Axelson	
5.		
6.		

Course Outcome and Program Outcome Mapping

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10
CO 1	2	3	2							
CO 2			3							
CO 3	3		2		3					
CO 4						2	3	3	2	
CO 5										
CO6										

Level of Mapping as: Low 1, Moderate 2, High 3

Class, Part & Semester	**:**	**First Year M. Tech (E&TC), Part I, Sem-II**					
Course Title	**:**	**Advance Mobile Systems**			***Course Code*:**	**:**	METCC23
Teaching Scheme (Hours)	**:**	Lecture :	3 Hrs/week		***Total Credits***	**:**	3
		Tutorial :	-- Hrs/week				
Evaluation Scheme (Marks)	**:**	ISE=40	ESE = 60	Grand Total=100	***Duration of ESE***	**:**	3 hrs

Revision:	**:**	Fourth	***Month***	**:**	July 2025
Pre-requisites *(if any)*	**:**	1. Principles of Signals and Systems 2. Principles of Communication Systems 3. Fundamentals of wireless communication			
Course Domain	**:**				

Course Rationale: *This course aims to impart a fundamental level understanding of sixth-generation (6G) wireless technology, encompassing its underlying concepts, use cases, and architectural frameworks. Starting with the overview of the evolution of wireless systems and standards, participants will delve into the essential principles behind 6G technology. The course will also cover the basics of multi-input multi output (MIMO) technology used in 6G wireless standards, along with advanced concepts like, massive MIMO, intelligent reflective surfaces (IRS), holographic beamforming, and orbital angular momentum (OAM). The students will also learn about next generation multiple access technologies such as non-orthogonal multiple access (NOMA), rate-splitting multiple access (RSMA), and fundamental coding schemes such as Polar and low density parity check (LDPC) Codes. Further, this course will also introduce students to advanced network topology for 6G, such as non-terrestrial networks, underwater networks,optical wireless networks and AI/ML models for 6G networks and devices. Lastly, the course will also address forthcoming insights and potential technological advancements shaping the next generation of wireless communication systems.*

Course Objectives: The Course teacher will		***Course Outcomes:*** Students will be able to	
73.	Explain Current Wireless systems (WLAN, Cellular, Satellite, Optical etc.) & 6G paradigm shifts, 6G KPIs	73.	Understand WLAN, Cellular, Satellite, Optical etc. & 6G paradigm shifts, 6G KPIs
74.	Explain SIMO and MISO systems, MIMO systems & Massive MIMO systems	74.	Understand MIMO systems
75.	Explain Metasurfaces, Holographic beamforming, Orbital Angular Momentum (OAM)	75.	Learn Intelligent reflective surfaces (IRS)/ Metasurfaces, Holographic Beamforming, Orbital Angular Momentum (OAM)
76.	Explain 6G modulation, channel coding	76.	Learn LDPC , Turbo Codes NOMA, OFDMA
77.	Explain Underwater Networks, Optical-Wireless Network	77.	Learn Underwater Networks, Optical-Wireless Network
78.	Explain Green Communication Network, AI / ML Models for 6G Networks and Devices	78.	Learn Green Communication Network AI / ML Models for 6G Networks and Devices

Curriculum Content	**Hours**
Unit I Overview of next-generation Communication System, Fundamentals of Wireless Communications , Evolution of Wireless Systems and Standards, Current Wireless systems (WLAN, Cellular, Satellite, Optical etc.), 6G paradigm shifts, use cases, 6G KPIs	6
Unit II Advanced MIMO Techniques, SIMO and MISO systems, MIMO systems, Massive MIMO systems	7
Unit III Intelligent reflective surfaces (IRS)/ Metasurfaces, Holographic Beamforming' Orbital Angular Momentum (OAM)	
Unit IV Modulation, Channel Coding and Multiple Access for 6G ,6G Coding Schemes (LDPC and Turbo Codes),6G Modulation Techniques, Multiple Access Schemes for 6G, Candidate waveforms for 6G: OFDM, NOMA, OFDMA	7
Unit V Advanced Network Topology for 6G,Non-Terrestrial Networks,Underwater Networks', Optical-Wireless Network	7
Unit VI Green Communication Network,AI / ML Models for 6G Networks and Devices	6
Suggested list of Tutorials and Assignments: As suggested by course teacher	

Suggested Text Books:	
1.	Paulo Sergio Rufino Henrique; Ramjee Prasad, ""6G The Road to the Future Wireless Technologies 2030,"", River Publishers, 2021,
2.	
Suggested Reference Books:	
1.	IEEE Communications, Wireless Communications Journals, Magazines, Tutorials papers
2.	3GPP standards
3.	6G enabling Technologies for next generation, by Amit Kumar Tyagi, Shrikant Tiwari, Shivani Gupta, Anand Kumar Mishra
4.	

Course Outcome and Program Outcome Mapping

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10
CO 1	1	2	2		1	1	1	1		
CO 2	2	3	3	1	1	1	1	1		
CO 3	2	2	2	2	1	1	1	1		
CO 4	2	2	2	1	1	1	1	1		
CO 5	2	2	2	1	1	1	1	1		

CO6		3	3	1	1	1	1	1		

Level of Mapping as: Low 1, Moderate 2, High 3

Elective-III

Class, Part & Semester	**:**	**First Year M. Tech (E&TC), Part I, Sem-I**					
Course Title	**:**	**SOC Design (Elective-III)**			***Course Code*:**	**:**	METCE21
Teaching Scheme (Hours)	**:**	Lecture :	3 Hrs/week		***Total Credits***	**:**	3
		Tutorial :	-- Hrs/week				
Evaluation Scheme (Marks)	**:**	ISE=40	ESE = 60	Grand Total=100	***Duration of ESE***	**:**	3 hrs
Revision:	**:**	Fourth			***Month***	**:**	July 2025
Pre-requisites *(if any)*	**:**	Digital circuit design and Programming language ‗C'is essential.					
Course Domain	**:**	Embedded					

Course Rationale: SoC design is crucial for creating compact, efficient, and cost-effective electronic devices, used in various applications like smartphones, embedded systems, and consumer electronics.SoC design involves integrating multiple components, such as processors, memory, and peripherals, onto a single chip.

Course Objectives:		***Course Outcomes:*** Students will be able to	
79.	To explain the System Architecture and Processor Architecture, Processor, Micro Architecture and approach for a SoC Design	79.	Understand the concept of system on chip and significance of SoC design and Modelling.
80.	To provide knowledge of Hardware and Software Design flow of SoC Design	80.	Design FSMD and Micro-programmed architectures for digital applications.
81.	To demonstrate use of Verilog for design of SoC based real time application	81.	Analyze the performance measures of SoC circuits and processor architectures. .
82.		82.	Analyze the impact of Platform-Centric Soc Design Approach.
83.		83.	Understand recent trends in Soc Prototyping, Testing and Verification
84.		84.	Design digital circuits, FSMD and Micro-programmed architectures using Verilog programming

Curriculum Content	**Hours**
Unit I Basic Concepts of SoC: The nature of hardware and software, data flow modelling and implementation, the need for concurrent models, analyzing synchronous data flow graphs, control flow modelling and the limitations of data flow models	7
Unit II FSM Datapath and Controller : Software and hardware implementation of data flow, analysis of control flow and data flow, Finite State Machine with data-path, cycle based bit parallel hardware, hardware model, FSM Data-path (FSMD), limitations of FSMD. Micro-programmed Architecture: Micro-programmed : control, encoding, data-path, Microprogrammed machine implementation, SOC modelling, hardware/software interfaces	5
Unit III Processor Architectures: Basic concepts in Processor Architecture, More Robust Processors such as Vector Processors, VLIW Processors and Superscalar Processors, Processor Selection for SOC, Memory Design. A SOC controller for digital still camera, portable multimedia system, SoC Platforms OMAP 137, PSoC 3 and PSoC 5	5
Unit IV Platform-Centric Soc Design Methodology: Introduction To Platforms, Platform-Based Design For Embedded Soc Systems, PlatformCentric Soc Design Approach, Comparison With Current Approaches.	8
Unit V Soc Prototyping And Verification : Soft Prototyping: Soc Design Flow, Transaction Level Modeling, Hw-Sw Co-Verification, HDL Simulator With HDL Processor Model, Hard Prototyping: Classification Of Hard Prototyping, Requirements Of Hard Prototyping, Examples Of Conventional Hard Prototyping System, Issues On Hardware/Software Co-Emulation Soc Testing And Design For Testability: Test Access Control System (TACS), A Typical Soc Test Design Flow, A Tacs-Based Soc Architecture, Test Integration Issues And Solutions, STEAC: Soc Test Aid Console, BRAINS	7
Unit VI Digital Circuit Design using Verilog: Gate Level Modeling: Introduction, AND Gate Primitive, Module Structure, Other Gate Primitives, Illustrative Examples, Tristate Gates, Array of Instances of Primitives, Design of Flip-Flops with Gate Primitives Modeling at Dataflow Level: Introduction, Continuous Assignment Structure, Delays and Continuous Assignments, Assignment to Vector, Operators. Switch Level Modeling: Basic Transistor Switches, CMOS Switches, Bidirectional Gates, Time Delays with Switch Primitives, instantiation with strengths and delays, Switch level modeling for NAND, NOR and XOR.	8

Suggested list of Tutorials and Assignments: As suggested by the course teacher	
Suggested Text Books:	
1.	Hubert Kaeslin, "Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication", Cambridge University Press, 2008.
2.	B. Al Hashimi, "System on chip-Next generation electronics", The IET, 2006
3.	Vijay Madisetti, Chonlameth Arpnikanondt, A Platform-Centric Approach to System-on-Chip (SOC) Design (2004)
Suggested Reference Books:	
1.	Rochit Rajsuman, "System-on- a-chip: Design and test", Advantest America R&D Center, 2000
2.	P Mishra and N Dutt, "Processor Description Languages", Morgan Kaufmann, 2008
3.	Michael J. Flynn and Wayne Luk, "Computer System Design: System-on-Chip". Wiley, 2011
4.	JariNurmi, Processor Design - System-on-Chip Computing for ASICs and FPGAs (2007)
5.	
6.	

Course Outcome and Program Outcome Mapping

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10
CO 1										
CO 2	3	3								
CO 3				2						
CO 4			2							
CO 5	2	2								
CO6		2				2				

Level of Mapping as: Low 1, Moderate 2, High 3

Class, Part & Semester	**:**	**First Year M. Tech (E&TC), Part I, Sem-II**				
Course Title	**:**	**Multimedia Technologies (Elective-III)**		***Course Code*:**	**:**	METCE22
Teaching Scheme (Hours)	**:**	Lecture :	3 Hrs/week	***Total Credits***	**:**	3
		Tutorial :	-- Hrs/week			

Evaluation Scheme (Marks)	**:**	ISE=40	ESE = 60	Grand Total=100	***Duration of ESE***	**:**	3 hrs
Revision:	**:**	Fourth			***Month***	**:**	July 2025
Pre-requisites *(if any)*	**:**	**Signal Processing**					
Course Domain	**:**	**Image and Video**					

Course Rationale: A multimedia technology course aims to equip students with knowledge and skills in creating and managing multimedia content, including text, images, audio, video, and animation, with the goal of developing professionals capable of creating engaging and effective multimedia experiences.

Course Objectives:		***Course Outcomes:*** Students will be able to	
85.	Develop proficiency in using multimedia software for creating and editing various media elements.	85.	Understand the fundamentals of multimedia, including different media types, their characteristics, and applications.
86.	Prepare students for careers in multimedia, web design, animation, video production, and related fields.	86.	Learn about multimedia software and tools for content creation, editing, and publishing
87.	Develop skills for creating engaging and interactive content for various platforms, including online platforms and social media	87.	Understand theoretical aspects of multimedia and develop practical abilities for content creation, editing, and visual effects.
88.		88.	Enhance creative skills in designing engaging and effective multimedia content.
89.		89.	Learn to manage and organize multimedia projects efficiently.
90.		90.	Develop skills in digital media content development, ranging from graphic design to e-publishing.

Curriculum Content	**Hours**
Unit I Introduction to Multimedia - Characteristics of multimedia presentation - Multimedia Components - Digital representation - media and data stream- Multimedia documents-task-production-sharing and distribution- Properties of a Multimedia system.	7
Unit II	6

Multimedia Architectures , User Interfaces - OS Multimedia Support - Multimedia Extensions - Hardware Support - Distributed Multimedia Applications - Real Time Protocols .	
Unit III Play Back Architectures - Synchronization - Document architecture - Hypermedia Concepts - Hypermedia Design - Digital Copyrights - Digital Library - Multimedia Archives.	6
Unit IV Compression types and techniques - CODEC ;Text Compression - GIF coding standards; Audio Compression - ADPCM ; JPEG standards - JPEG 2000 compression - H.261 ; MPEG- MPEG 3- MPEG 7- MPEG 21 .	7
Unit V Multimedia Communication & Applications : Tele Services - Implementation of Conversational Services - Messaging Services - Retrieval Services - Tele Action Services - Tele Operation Services - Media Consumption - Media Entertainment - Virtual Reality**.**	7
Unit VI Instructional Activity , Simulation Using: Editing Tools - Image - sound- video; Painting and drawing Tools - 3D Modeling and animation Tools.	7
Suggested list of Tutorials and Assignments: As suggested by the course teacher	

Suggested Text Books:	
1.	
Suggested Reference Books:	
1.	Ralf Steinmetz, Klara Nahrstedt, "Multimedia Computing, Communications, and Applications", Pearson India, 2009..
2.	Ranjan Parekh, "Principles of Multimedia", Second Edition, McGraw Hill Education, 2017
3.	Ralf Steinmetz, Klara Nahrstedt, "Multimedia Systems", Springer, 2004.
4.	Tay Vaughan, "Multimedia: Making it Work", McGraw – Hill Education, Ninth Edition, 2014.
5.	Jerry D. Gibson, Toby Berger, Tom Lookabaugh, Dave Lindergh, Richard L. "Baker Digital Compression for Multimedia: Principles and Standards", Elsevier, 2006.
6.	

Course Outcome and Program Outcome Mapping

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10
CO 1		3								
CO 2		2	3							
CO 3				2						
CO 4	2		2							
CO 5		2								
CO6			2			2				

Level of Mapping as: Low 1, Moderate 2, High 3

Class, Part & Semester	**:**	**First Year M. Tech (E&TC), Part I, Sem-II**					
Course Title	**:**	**Robotics and Automation (Elective-III)**			***Course Code*:**	**:**	METCE23
Teaching Scheme (Hours)	**:**	Lecture :	3 Hrs/week		***Total Credits***	**:**	3
		Tutorial :	-- Hrs/week				
Evaluation Scheme (Marks)	**:**	ISE=40	ESE = 60	Grand Total=100	***Duration of ESE***	**:**	3 hrs
Revision:	**:**	Fourth			***Month***	**:**	July 2025
Pre-requisites *(if any)*	**:**	**Microcontroller based systems**					
Course Domain	**:**	**Automation**					

Course Rationale: A Robotics and Automation course typically aims to equip students with fundamental knowledge and practical skills in robotics and automation, enabling them to understand robot configurations, kinematics, dynamics, programming, and applications in various industries. s

Course Objectives:		***Course Outcomes:*** Students will be able to	
91.	To impart the knowledge of the fundamentals in robotics and automation.	**91.**	Explain 3D translation and orientation representation & Illustrate the robot arm kinematics and use of Robot Operating System usage.
92.	To understand the components of robot end effectors, material handling and automation.	**92.**	Design / Simulate a robot which meets kinematic requirements.
93.	To choose gripper type, product design considerations for automated assembly and solve gripper force.	**93.**	Apply localization and mapping aspects of mobile robotics. 4
94.		**94.**	understand ROS applications
95.		**95.**	understand robot programming
96.		**96.**	

Curriculum Content	**Hours**
Unit I Introduction: Definitions, Types of Robots, Application of Robots, Representing Position and Orientation, Representing Pose in 2-Dimensions, Representing Pose in 3-Dimensions, Representing Orientation in 3-Dimensions, Combining Translation and Orientation.	6
Unit II Time and Motion: Trajectories, Smooth One-Dimensional Trajectories, Multi-Dimensional Case, Multi-Segment Trajectories, Interpolation of Orientation in 3D, Cartesian Motion, Time Varying Coordinate Frames, Rotating Coordinate Frame, Incremental Motion, Inertial Navigation Systems. Mobile Robot Vehicles, Mobility, Car-like Mobile Robots, Moving to a Point, Following a Line, Following a Path, Moving to a Pose.	6
Unit III Navigation: Reactive Navigation, Braitenberg Vehicles, Simple Automata, Map-Based Planning, Distance Transform, D*, Voronoi Roadmap Method, Probabilistic Roadmap Method,Localization, Dead Reckoning, Modeling the Vehicle, Estimating Pose, Using a Map, Creating a Map, Localization and Mapping, Monte-Carlo Localization	7
Unit IV Robot Arm Kinematics: Describing a Robot Arm, Forward Kinematics, A 2-Link Robot, A 6- Axis Robot, Inverse Kinematics, Closed-Form Solution, Numerical Solution, Under-Actuated Manipulator, Redundant Manipulator, Trajectories, Joint-Space Motion, Cartesian Motion, Motion through a Singularity.	7
Unit V Getting Started with ROS: Installing ROS, Understanding the ROS Filesystem level, Packages, Stacks, Messages, Services, Understanding the ROS Computation Graph level, Nodes, Topics, Services, Messages, Bags, Master, Parameter Server, Creating workspace, Creating & Building an ROS package, Creating & Building the node, Visualization of images, Working with stereo vision, 3D visualization, Visualizing data on a 3D world using rviz	7
Unit VI Robot Programming : Using Sensors and Actuators with ROS, SCORBOT structure, joint movements, work envelop, motors, encoders, microswitch, transmission, gripper, SCORBOT programming, IS-14533 : 2005 Manipulating industrial robots - Performance criteria related test methods, Mobile Robot Programming, Industrial Robot Programming**.**	7
Suggested list of Tutorials and Assignments: As suggested by the course teacher	

Suggested Text Books:	
1.	Robotics, Vision and Control: Fundamental Algorithms in MATLAB® - Peter Corke, Springer Tracts in Advanced Robotics, Volume 73, 2011
2.	Learning ROS for Robotics Programming - Aaron Martinez & Enrique Fernández, Packt Publishing, September 2013
3.	
Suggested Reference Books:	
1.	Robotics for Engineers -YoramKoren, McGraw Hill International, 1st edition, 1985..
2.	Industrial Robotics-Groover, Weiss, Nagel, McGraw Hill International, 2nd edition, 2012
3.	Robotics, control vision and intelligence-Fu, Lee and Gonzalez. McGraw Hill International, 2nd edition, 2007.
4.	Introduction to Robotics- John J. Craig, Addison Wesley Publishing, 3rd edition, 2010.
5.	
6.	

Course Outcome and Program Outcome Mapping

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10
CO 1			2							
CO 2	2	3			2					
CO 3		2	3		2	3				
CO 4	3	3		2	3					
CO 5		2		3	3	1				
CO6										

Level of Mapping as: Low 1, Moderate 2, High 3

Class, Part & Semester	**:**	**First Year M. Tech (E&TC), Part I, Sem-II**					
Course Title	**:**	**Advanced Computer Architecture (Elective-III)**			***Course Code*:**	**:**	METCE24
Teaching Scheme (Hours)	**:**	Lecture :	3 Hrs/week		***Total Credits***	**:**	3
		Tutorial :	-- Hrs/week				
Evaluation Scheme (Marks)	**:**	ISE=40	ESE = 60	Grand Total=100	***Duration of ESE***	**:**	3 hrs
Revision:	**:**	Fourth			***Month***	**:**	July 2025

Pre-requisites *(if any)*	**:**	**Processor Architecture**
Course Domain	**:**	**Computing Techniques**

Course Rationale: An Advanced Computer Architecture course aims to provide a deep understanding of modern computer systems, focusing on performance analysis, advanced processor architectures, and memory hierarchy design, enabling students to analyze, design, and optimize computer systems.

Course Objectives:		***Course Outcomes:*** Students will be able to	
97.	To make students know about the Parallelism concepts in Programming	97.	Demonstrate concepts of parallelism in hardware/software.
98.	To give the students an elaborate idea about the different memory systems and buses.	98.	Discuss memory organization and mapping techniques.
99.	To introduce the advanced processor architectures to the students.	99.	Describe architectural features of advanced processors.
100.	To make the students know about the importance of multiprocessor and multicomputers.	100.	Interpret performance of different pipelined processors.
101.	To study about data flow computer architectures	101.	Explain data flow in arithmetic algorithms
102.		102.	Development of software to solve computationally intensive problems

Curriculum Content	**Hours**
Unit I ILP – Concepts and challenges – Hardware and software approaches – Dynamic scheduling – Speculation - Compiler techniques for exposing ILP – Branch prediction	6
Unit II VLIW & EPIC – Advanced compiler support – Hardware support for exposing parallelism – Hardware versus software speculation mechanisms – IA 64 and Itanium processors – Limits on ILP.	7
Unit III Symmetric and distributed shared memory architectures – Performance issues – Synchronization – Models of memory consistency – Introduction to Multithreading.	6
Unit IV Cache performance – Reducing cache miss penalty and miss rate – Reducing hit time – Main memory and performance – Memory technology. Types of storage devices – Buses – RAID – Reliability, availability and dependability – I/O performance measures – Designing an I/O system.	7
Unit V Software and hardware multithreading – SMT and CMP architectures – Design issues	6

Unit VI Case studies – Intel Multi-core architecture – SUN CMP architecture - heterogenous multi-core processors – case study: IBM Cell Processor	7
Suggested list of Tutorials and Assignments: As suggested by the course teacher	
Suggested Text Books:	
1.	John L. Hennessey and David A. Patterson, " Computer architecture – A quantitative approach", Morgan Kaufmann / Elsevier Publishers, 4th. edition, 2007.
2.	
3.	
Suggested Reference Books:	
1.	David E. Culler, Jaswinder Pal Singh, "Parallel computing architecture: A hardware/software approach" , Morgan Kaufmann /Elsevier Publishers, 1999.
2.	Kai Hwang and Zhi.WeiXu, "Scalable Parallel Computing", Tata McGraw Hill, New Delhi, 2003.
3.	

Course Outcome and Program Outcome Mapping

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10
CO 1		3	3							
CO 2		2	2							
CO 3				2						
CO 4			2						2	
CO 5		2	2							
CO6						2				

Level of Mapping as: Low 1, Moderate 2, High 3

Elective -IV

Class, Part & Semester	**:**	**First Year M. Tech (E&TC), Part I, Sem-II**				
Course Title	**:**	**MIMO System (Elective -IV)**		***Course Code*:**	**:**	METCOE21
Teaching Scheme	**:**	Lecture :	3 Hrs/week	***Total Credits***	**:**	3
		Tutorial :	-- Hrs/week			

(Hours)							
Evaluation Scheme (Marks)	**:**	ISE=40	ESE = 60	Grand Total=100	***Duration of ESE***	**:**	3 hrs
Revision:	**:**	Fourth			***Month***	**:**	July 2025
Pre-requisites *(if any)*	**:**	**Digital Communications, Signals and Systems, Wireless communications**					
Course Domain	**:**	**Communication**					

Course Rationale: To learn about MIMO communication systems, capacity of MIMO, space time coding scheme and MIMO in 4G/5G wireless communications with available technology and schemes

Course Objectives: The Course teacher will		***Course Outcomes:*** Students will be able to	
103.	Impart in depth knowledge about MIMO	103.	Understand SIMO, MISO, MIMO in-depth
104.	Impart in depth knowledge about MIMO channel capacity	104.	Understand random MIMO channels, Capacity of i.i.d., Rayleigh fading MIMO channels capacity.
105.	Impart in depth knowledge about *Space-Time codes*	105.	Understand Alamouti space-time codes, Space-time block codes, Space-time trellis codes, Space-time turbo codes.
106.	Impart in depth knowledge about *MIMO detection, Advances in MIMO wireless communication*	106.	Understand *MIMO detection, Advances in MIMO wireless communication,* Spatial modulation, cognitive radio, multiuser MIMO, MIMO systems for 5G wireless.
107.		**107.**	

Curriculum Content	**Hours**
Unit I *Introduction*: Diversity-multiplexing trade-off, transmit diversity schemes, advantages and applications of MIMO systems	6
Unit II *Analytical MIMO channel models*: Uncorrelated, fully correlated, separately correlated and keyhole MIMO fading models, parallel decomposition of MIMO channel. *Power allocation in MIMO systems*: Uniform, adaptive and near optimal power allocation.	7
Unit III *MIMO channel capacity*: Capacity for deterministic and random MIMO channels, Capacity of i.i.d., separately correlated and keyhole Rayleigh fading MIMO channels.	6

Unit IV *Space-Time codes*: Advantages, code design criteria, Alamouti space-time codes, SER analysis of Alamouti space-time code over fading channels, Space-time block codes, Space-time trellis codes, Performance analysis of Space-time codes over separately correlated MIMO channel, Space-time turbo codes.	7
Unit V *MIMO detection*: ML, ZF, MMSE, ZF-SIC, MMSE-SIC, LR based detection	7
Unit VI *Advances in MIMO wireless communications*: Spatial modulation, MIMO based cooperative communication and cognitive radio, multiuser MIMO, cognitive-femtocells and large MIMO systems for 5G wireless.	6
Suggested list of Tutorials and Assignments: As suggested by the course teacher	
Suggested Text Books:	
1.	
2.	
Suggested Reference Books:	
1.	B. Clerckx and C. Oestges, MIMO wireless networks, Elsevier Academic Press, 2nd ed., 2013.
2.	T. M. Duman and A. Ghrayeb, Coding for MIMO communication systems, John Wiley and Sons, 2007.
3.	N. Costa and S. Haykin, Multiple-input multiple-output channel models, John Wiley & Sons, 2010.
4.	J. Choi, Optimal Combining & Detection, Cambridge University Press, 2010.
5.	A. Chokhalingam and B. S. Rajan, Large MIMO systems, Cambridge University Press, 2014.
6.	

Course Outcome and Program Outcome Mapping

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10
CO 1	3	1	1	1	1	1	1	1		
CO 2	2	1	1	1	1	1	1	1		
CO 3	2	1	1	1	1	1	1	1		
CO 4	3	1	1	1	1	1	1	1		
CO 5										
CO6										

Level of Mapping as: Low 1, Moderate 2, High 3

Class, Part & Semester	**:**	**First Year M. Tech (E&TC), Part I, Sem-II**					
Course Title	**:**	**Satellite Communication (Elective -IV)**			***Course Code*:**	**:**	METCOE22
Teaching Scheme (Hours)	**:**	Lecture :	3 Hrs/week		***Total Credits***	**:**	3
		Tutorial :	-- Hrs/week				
Evaluation Scheme (Marks)	**:**	ISE=40	ESE = 60	Grand Total=100	***Duration of ESE***	**:**	3 hrs
Revision:	**:**	Fourth			***Month***	**:**	July 2025
Pre-requisites *(if any)*	**:**	Satellite communication					
Course Domain	**:**	Communication					

Course Rationale: This course provides an introduction to the fundamentals of orbital mechanics and launchers, link budgets, modulation, coding, multiple access techniques, propagation effects, and earth terminals. This course provides an understanding how analog and digital technologies are used for satellite communications networks. They will gain skills for performance improvement for different available satellites by calculating power Budgets

Course Objectives: The Course teacher will		***Course Outcomes:*** Students will be able to	
108.	Impart in depth knowledge of orbital mechanism.	**108.**	Visualize the architecture of satellite systems as a means of high speed, high range communication system.
109.	Impart in depth knowledge of link budgets, modulation, coding, multiple access techniques, propagation effects, and earth terminals.	**109.**	State various aspects related to satellite systems such as orbital equations, sub-systems in a satellite, link budget, modulation and multiple access schemes.
110.	Impart in depth knowledge power budget.	**110.**	Solve numerical problems related to orbital motion and design of link budget for the given parameters and conditions.
111.		**111.**	
112.		**112.**	
113.		**113.**	

Curriculum Content	**Hours**
Unit I Architecture of Satellite Communication System: Principles and architecture of satellite	6

Communication, Brief history of Satellite systems, advantages, disadvantages, applications, and frequency bands used for satellite communication and their advantages/drawbacks	
Unit II Orbital Analysis: Orbital equations, Kepler's laws of planetary motion, Apogee and Perigee for an elliptical orbit, evaluation of velocity, orbital period, angular velocity etc of a satellite, concepts of Solar day and Sidereal day.	7
Unit III Satellite sub-systems: Architecture and Roles of various sub-systems of a satellite system such as Telemetry, tracking, command and monitoring (TTC & M), Attitude and orbit control system (AOCS), Communication sub-system, power sub-systems, antenna sub-system.	7
Unit IV Typical Phenomena in Satellite Communication: Solar Eclipse on satellite, its effects, remedies for Eclipse, Sun Transit Outage phenomena, its effects and remedies, Doppler frequency shift phenomena and expression for Doppler shift.	7
Unit V Satellite link budget: Flux density and received signal power equations, Calculation of System noise temperature for satellite receiver, noise power calculation, Drafting of satellite link budget and C/N ratio calculations in clear air and rainy conditions, Case study of Personal Communication system (satellite telephony) using LEO.	7
Unit VI Modulation and Multiple Access Schemes used in satellite communication.Typical case studies of VSAT, DBS-TV satellites and few recent communication satellites launched by NASA/ ISRO. GPS.	6
Suggested list of Tutorials and Assignments: As suggested by course teacher	
Suggested Text Books:	
1.	
Suggested Reference Books:	
1.	Timothy Pratt and Others, "Satellite Communications", Wiley India, 2nd ¬ edition,2010.
2.	S. K. Raman, "Fundamentals of Satellite Communication", PearsonEducation India, 2011.
3.	Tri T. Ha, "Digital Satellite Communications", Tata McGraw Hill, 2009
4.	Dennis Roddy, "Satellite Communication", McGraw Hill, 4th Edition, 2008

Course Outcome and Program Outcome Mapping

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10
CO 1	2	1	1	1	1	1	1	1		
CO 2	2	1	1	1	1	1	1	1		
CO 3	2	1	1	1	1	1	1	1		
CO 4										
CO 5										

CO6										

Level of Mapping as: Low 1, Moderate 2, High 3

Class, Part & Semester	**:**	**First Year M. Tech (E&TC), Part I, Sem-II**					
Course Title	**:**	**Smart and Phase Array Antenna Design (Elective -IV)**			***Course Code*:**	**:**	METCOE23
Teaching Scheme (Hours)	**:**	Lecture :	3 Hrs/week		***Total Credits***	**:**	3
		Tutorial :	-- Hrs/week				
Evaluation Scheme (Marks)	**:**	ISE=40	ESE = 60	Grand Total=100	***Duration of ESE***	**:**	3 hrs
Revision:	**:**	Fourth			***Month***	**:**	July 2025
Pre-requisites *(if any)*	**:**	**Antenna theory**					
Course Domain	:	**Communication**					

Course Rationale*:* In this course students shall learn basics as well as advanced phase are antennas. they shall learn radiation pattern of two point sources, Dolf Tchebyschef array, Pattern Synthesis for Linear and Planar Arrays, Methods of Pattern Optimization/Adaptive Arrays, various antennas and their feed mechanism,

Course Objectives: The Course teacher will		***Course Outcomes:*** Students will be able to	
114.	Teach radiation pattern of two point sources for various distances and phases.	114.	Shall understand how to obtain radiation pattern of two point sources for various cases.
115.	Teach Pattern Synthesis for Linear and Planar Arrays	115.	understand Pattern Synthesis for Linear and Planar Arrays
116.	Teach Adaptive antennas	116.	Understand Adaptive antennas.

117.	Teach various antennas and their feed mechanism for array antenna design	117.	Understand various antennas and their feed mechanism for array antenna design
118.		**118.**	
119.		**119.**	

Curriculum Content	**Hours**
Unit I Array of two point sources, Linear broadside array with nonuniform amplitude distributions, Dolf Tchebyscheff distribution	6
Unit II Pattern Synthesis for Linear and Planar Arrays Linear Arrays and Planar Arrays with Separable Distributions, Fourier Transform Method, Schelkunov's (Schelkunoff's) Form, Woodward Synthesis, Dolph-Chebyshev Synthesis, Taylor Line Source Synthesis, Modified sin pz/pz Patterns, Bayliss Line Source Difference Patterns.	7
Unit III Methods of Pattern Optimization/Adaptive Arrays Pattern Optimization, Adaptive Arrays, Generalized S/N Optimization for Sidelobe Cancelers, Phased and Multiple-Beam Arrays, Operation as Sidelobe Canceler, Fully Adaptive Phased or Multiple-Beam Arrays, Wideband Adaptive Control	6
Unit IV Elements for Phased Arrays, Array Elements, Polarization Characteristics of Infinitesimal Elements in Free Space, Electric Current (Wire) Antenna Elements, Effective Radius of Wire Structures with Noncircular Cross Section, The Dipole and the Monopole, Special Feeds for Dipoles and Monopoles, Dipoles Fed Off-Center, The Sleeve Dipole and Monopole, The Bowtie and Other Wideband Dipoles, The Folded Dipole , Microstrip Dipoles, Other Wire Antenna Structures, Broadband Flared-Notch, Vivaldi, and Cavity-Backed Antennas, Aperture Antenna Elements, Slot Elements, Waveguide Radiators, Ridged Waveguide Elements, Horn Elements, Microstrip Patch Elements, Microstrip Patch, The Balanced Fed Radiator of Collings Elements for Alternative Transmission Lines, Elements and Row (Column) Arrays for One-Dimensional Scan, Waveguide Slot Array Line Source Elements, Printed Circuit Series-Fed Arrays, Elements and Polarizers for Polarization Diversity	7
Unit V Special Array Feeds for Limited Field-of-View and Wideband Arrays Multiple-Beam Systems, Beam Crossover Loss, Orthogonality Loss and the Stein Limit, Multiple-Beam Matrices and Optical Beamformers, Antenna Techniques for Limited Field-of-View Systems, Minimum Number of Controls, Periodic and Aperiodic Arrays for Limited Field of View,	7
Unit VI Constrained Network for Completely Overlapped Subarrays, Reflectors and Lenses with Array Feeds, Practical Design of a Dual-Transform System, Wideband	7

Scanning Systems, Broadband Arrays with Time-Delayed Offset Beams, Contiguous Time-Delayed Subarrays for Wideband Systems, Overlapped Time-Delayed Subarrays for Wideband Systems	

Suggested list of Tutorials and Assignments: As suggested by the course teacher

Suggested Text Books:	
1.	
2.	
3.	
Suggested Reference Books:	
1.	Phased array antenna hand book by Robbert J. Mailbox
2.	
3.	
4.	
5.	
6.	

Course Outcome and Program Outcome Mapping

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10
CO 1	1	1	1	1	1		1	1		
CO 2	1	1	1	1	1	1	1	1		
CO 3	1	1	1	1	1	1	1	1		
CO 4	1	1	1	1	1	1	1	1		
CO 5										
CO6										

Level of Mapping as: Low 1, Moderate 2, High 3

Class, Part & Semester	:	**First Year M. Tech (E&TC), Part I, Sem-II**				
Course Title	:	**Seminar-II**		***Course Code*:**	:	METCC 24
Teaching Scheme (Hours)	:	Practical :	2 Hrs/week	***Total Credits***	:	1

Evaluation Scheme (Marks)	**:**	/IOE= 50 Marks	EOE= ---	Total= 50 marks	***Duration of EPE***	**:**	----
Revision:	**:**	Fourth			***Month***	**:**	July 2025
Pre-requisites *(if any)*	**:**	**Advance Technology Studies**					
Course Domain	**:**	**Technology Exchange**					
Course Rationale: Students should get acquainted with the advance topics in the field of Electronic, IT , E&TC and Computer Engineering							

Course Objectives: The Course teacher will		***Course Outcomes:*** Students will be able to	
1.	*To encourage students for research development*	1	*Demonstrate and explore New Technology*
2.		2	*Inculcate ability to make presentation*
3.		3.	*Explore the research*
4.		4	*Inculcate innovations*
5			
6.			

Course Outcome and Program Outcome Mapping

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10
CO 1	2				3				3	
CO 2		3					2			
CO 3				2	2				2	
CO 4			3			2				2
CO 5	2									
CO6										

Level of Mapping as: Low 1, Moderate 2, High 3

Class, Part & Semester	**:**	**First Year M. Tech (E&TC), Part I, Sem-II**				
Course Title	**:**	**Laboratory-I : Real Time Operating System Lab**		***Course Code*:**	**:**	METCCC25
Teaching Scheme (Hours)	**:**	Practical :	2 Hrs/week	***Total Credits***	**:**	1

Evaluation Scheme (Marks)	**:**	IOE=50 marks	EOE= ---	Total=50 marks	***Duration of EPE***	**:**	----
Revision:	**:**	Fourth			***Month***	**:**	July 2025
Pre-requisites *(if any)*	**:**	Operating system and Embedded System					
Course Domain	**:**	Embedded System					

Course Rationale: Please write it in 3 to 4 lines

Course Objectives:		***Course Outcomes:*** Students will be able to	
1.	***To Introduce the students about Operating Systems and acquainting students to Real Time Operating Systems***	**1.**	***Comprehend the basic components of an operating system***
2.	***To teach the students about Task Management and Enabling students to understand RTOS Scheduling***	**2.**	***Learn about the basics of real-time concepts***
3.	***To Introdu the students about interprocess communication and Memory Management***	**3.**	***Acquire knowledge about task management***
4.		**4.**	***Acquaint with RTOS scheduling***
5		**5.**	***Learn about IPC synchronization***
6.		**6.**	***Apply the knowledge for developing practical applications of modern real-time systems***

List of Experiments

Sr. No.	
1.	**Blinking LEDs:** Create tasks that control the blinking of different LEDs at different intervals.
2.	**Displaying Text on an LCD:** Develop tasks to display different messages or data on an LCD display.
3.	**Interfacing with a Sensor:** Read sensor data (e.g., temperature, pressure) and display it on an LCD or send it to a PC.
4.	**Controlling a Motor:** Control the speed and direction of a motor using RTOS tasks.
5.	**Implementing a Simple Game:** Develop a simple game using RTOS tasks for

	input handling, game logic, and output display.
6.	**Implementing a Simple Network Application:** Create tasks for sending and receiving data over a network using the RTOS.
7.	**Implementing a Real-Time Clock:** Create a task to keep track of time and display it on an LCD.
8.	**Implementing a Simple Operating System:** Create a simple operating system with basic features like process management, memory management, and I/O management.
9.	Interfacing of 7 segment Display
10.	Relay Interfacing
General Instructions: if any regarding course delivery and assessment	
Suggested Text Books/ Reference Books/Manual	
1.	Labrossy J. J, Lawrence, "µC/OS-II, The real time Kernel", R & D Publication.
2.	Tanenbaum A S, "Modern Operating Systems", Prentice Hall.
3.	Raj Kamal, "Embedded Systems Architecture, Programming and design", Tata McGraw-Hill
4.	

Course Outcome and Program Outcome Mapping

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10
CO 1										
CO 2	2	3			3					
CO 3				2		2	2			3
CO 4			2					2		
CO 5		2							1	
CO6		2			3	2				

Level of Mapping as: Low 1, Moderate 2, High 3

Class, Part & Semester	:	**First Year M. Tech (E&TC), Part I, Sem-II**				
Course Title	:	**Laboratory-II : Advance Mobile system lab**		***Course Code*:**	:	METCC 26
Teaching Scheme (Hours)	:	Practical :	2 Hrs/week	***Total Credits***	:	1

Evaluation Scheme (Marks)	:	IOE=50 marks	EPE/EOE= ---	Total= 50 marks	***Duration of EPE***	:	----
Revision:	:	Fourth			***Month***	:	July 2023
Pre-requisites *(if any)*	:	**mobile communication**					
Course Domain	:	**communication**					

Course Rationale: Please write it in 3 to 4 lines

Course Objectives: The Course teacher will		***Course Outcomes:*** Students will be able to	
1.	*Impart in depth knowledge on SIMO, MISO and MIMO systems*	1.	*Understand SIMO, MISO and MIMO systems*
2.	*Impart in depth knowledge on NOMA systems*	2.	*Understand NOMAsystems*
3.	*Impart in depth knowledge on OFDM systems*	3.	*Understand NOMAsystems*
4.	*Impart in depth knowledge on Green Technology*	4.	*Understand Green Technology*
5		5.	
6.		6.	

List of Experiments

Sr. No.	
1.	Simulation of SIMO
2.	Simulation of MISO
3.	Simulation of MIMO
4.	Simulation of NOMA
5.	Simulation of OFDM
6.	Explain Green Technology
7.	
8.	
9.	
10.	
11.	
12.	

Suggested Text Books/ Reference Books/Manual

1.	Paulo Sergio Rufino Henrique; Ramjee Prasad, ""6G The Road to the Future Wireless Technologies 2030,"", River Publishers, 2021,
2.	
3.	
4.	

Course Outcome and Program Outcome Mapping

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10
CO 1	2	2	2	1	1			1		
CO 2	2	2	2	1	1			1		
CO 3	2	2	2	1	1			1		
CO 4	2	2	2	1	1			1		
CO 5										
CO6										

Level of Mapping as: Low 1, Moderate 2, High 3

SHIVAJI UNIVERSITY, KOLHAPUR
Department of Technology
M. Tech. Electronics & Telecommunication Course Structure
Semester- III
Applicable From Academic Year 2025-26

Sr. No	Subject Code	Subject Title	Teaching Scheme (Hours/week)				Examination Scheme			
							Theory		Practical	
			L	T	P	Credits	Scheme	Max. marks	Scheme	Max. marks
2	METCC31	Industrial Training	-	-	2*	5**	--------	-------	IOE	50
									EOE	50
3	METCC32	Dissertation Phase-I	-	-	2*	15	--------	-------	IOE	100
									EOE	100
		Total	-	-	4	20				300
Total Contact hours per week =4*										

Industrial Training

Industrial Training of 8 Weeks at the end of first year OR Industrial Training will be split into two slots of Four weeks during semester III. Evaluation at the end of third semester on the basis of given report and presentation to concern guide.

Dissertation Phase-I

The student shall be allowed to submit the dissertation phase I report only after the completion of minimum 50% work of the total project with intermediate /partial results of the dissertation project to the concern guide and the dissertation phase II report only after the full-fledge demonstration of his /her work to the concerned guide. Assessment of the dissertation shall be based on design & implementation aspects, documentation & presentation skills, utility of the dissertation work & publications based on the same. For the dissertation phase I and phase II concern guide should guide to each student minimum for 2 hrs per week till the final submission of the dissertation of the concern student.

SHIVAJI UNIVERSITY, KOLHAPUR
Department of Technology
M. Tech. Electronics & Telecommunication Course Structure
Semester- IV
Applicable From Academic Year 2025-26

Sr. No.	Subject Code	Subject Title	Teaching Scheme (Hours/week)				Examination Scheme			
							Theory		Practical	
			L	T	P	Credits	Scheme	Max. marks	Scheme	Max. marks
1	METCC41	Dissertation Phase-II	-	-	4*	20	---	---	IOE	100
									EOE	200
		Total	-	-	4	20	--	---		300
Total Contact hours per week =4*										

*Students are expected to do self-study for two hours as per the guidance given by the dissertation guide Guide and report to the department as per the schedule in the disseminated time table.

During Dissertation Phase –II students are expected to complete their respective dissertation in all respect and submit it to the University for the Further Procedures.

Note:

** For dissertation guiding 2 hrs/week load will be considered for the designated dissertation guide (faculty member) of the program/department

Equivalence of M. Tech (Electronics) Pre-revised

The above detailed syllabus is a revised version of the M. Tech (Electronics) course being conducted by the Shivaji University at the Technology Department of the University. This syllabus is to be implemented from June 2025-26.

The Equivalence for the subjects of Electronics at M. Tech Semester I and II pre-revised course under the faculty of Engineering and Technology is as follows.

M. Tech (Electronics) Part-I Semester I

Sr. No	**M. Tech (Electronics) Semester I Pre-revised syllabus List of Courses for Equivalence**	**M. Tech (Electronics & Telecommunication) Semester I Revised syllabus courses equivalence with Pre-revised courses**	**Remark**
1.	Research Methodology (Audit)	Research Methodology	Two Credits assigned
2.	High Speed Analog Design	**Not Available**, New Course Introduced	**No equivalent** course available from revised course syllabus list
3.	Reconfigurable Platforms & HDL	Reconfigurable Computing	**Equivalent**; from open Elective-II Sem-I of revised course syllabus
4.	Communication Networks	Advance Computer Networks	**Equivalent**
5.	Elective-I Memory Technologies	**Not Available**, New Course Introduced	**No equivalent** course available from revised course syllabus list
6.	Elective-I CMOS VLSI Design	**Not Available**, New Course Introduced	**No equivalent** course available from revised course syllabus list

7.	Elective-I Asynchronous Circuit Design	**Not Available**, New Course Introduced	**No equivalent** course available from revised course syllabus list
8.	Elective-I Advanced Computer Architecture -	Advance Computer Architecture	**Equivalent;** from Elective-III Sem-2 of revised course syllabus list
9.	Elective-II (Open Elective) Digital System And Testing	VLSI Testing and Testability	**Equivalent;** from Elective-II Sem-1 of revised course syllabus list
10.	Elective-II (Open Elective) Mixed Signal ASIC Design	**Not Available**, New Course Introduced	**No equivalent** course available from revised course syllabus list
11.	Elective-II (Open Elective) Automotive Embedded Systems	**Not Available**, New Course Introduced	**No equivalent** course available from revised course syllabus list
12.	High Speed Analog Design Lab	**Not Available**, New Course Introduced	**No equivalent** course available from revised course syllabus list
13.	Reconfigurable Platforms & HDL Lab	**Not Available**, New Course Introduced	**No equivalent** course available from revised course syllabus list
14.	Communication Networks Lab	Advance Computer Networks Lab	**Equivalent**
15.	Seminar-I	Seminar-I	**Equivalent**

M. Tech (Electronics)-I Semester II

Sr. No	**M. Tech (Electronics) Semester II Pre-revised syllabus**	**M. Tech (Electronics & Telecommunication) Semester II Revised syllabus**	**Remark**
1.	DSP Processor	**Not Available**, New Course Introduced	**No equivalent** course available from revised course syllabus list
2.	Real Time Operating System	Real Time Operating Systems	**Equivalent**
3.	Mobile Computing	Advance Mobile System	**Equivalent**
4.	Elective-III System on Chip `	SoC Design	**Equivalent;** from Elective-III Sem-II of revised course syllabus list
5.	Elective-III Wavelet Transform and Applications	**Not Available**, New Course Introduced	**No equivalent** course available from revised course syllabus list
6.	Elective-III Micro Elctro Mechanical	**Not Available**, New Course Introduced	**No equivalent** course available from revised course syllabus list

	System		
7.	Elective-III Robotics and Machine Vision	Robotics and Automation	**Equivalent;** from Elective-III Sem-II of revised course syllabus list
8.	Elective-IV (Open Elective) RF Integrated Circuit Design	**Not Available**, New Course Introduced	**No equivalent** course available from revised course syllabus list
9.	Elective-IV (Open Elective) High Performance Networks	**Not Available**, New Course Introduced	**No equivalent** course available from revised course syllabus list
10.	Elective-IV (Open Elective) High Speed Digital Design	**Not Available**, New Course Introduced	**No equivalent** course available from revised course syllabus list
11.	DSP Processor Lab	**Not Available**, New Course Introduced	**No equivalent** course available from revised course syllabus list
12.	Real Time Operating System Lab	Real Time Operating Systems Lab	**Equivalent**
13.	Mobile Computing Lab	Advance Mobile System Lab	**Equivalent**
14.	Seminar-II	Seminar-II	**Equivalent**

M. Tech (Electronics) Part-II Semester III

Sr. No	M. Tech (Electronics) Semester III Pre-revised syllabus	M. Tech (Electronics & Telecommunication) Semester III Revised syllabus	Remark
1	Industrial Training	Industrial Training	**Equivalent**
2	Dissertation Phase-I	Dissertation Phase-I	**Equivalent**

M. Tech (Electronics) Part-II Semester IV

Sr. No	M. Tech (Electronics) Semester IV Pre-revised syllabus	M. Tech (Electronics & Telecommunication) Semester IV Revised syllabus	Remark
1	Dissertation Phase – II	Dissertation Phase-II	**Equivalent**